

Project Namel: Tahoe MT MLK

PCB Number: 15141-1

PCBA Ver.: A00

SCH Ver.: A00

Project Code : 3PD06M010001

PCB Size: 268.7 x 243.5mm, 1.6mm, 4 Layers

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73	(R)
74	(R)
75	(R)
76	(R)
77	(R)
78	(R)
79	(R)
80	(R)
81	(R)
82	(R)
83	(R)
84	(R)
85	(R)
86	(R)
87	(R)
88	(R)
89	(R)
90	(R)
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### Jumper Setting

JMP1	Pin 1-2	With Jumper to ME Disable
	Pin 3-4	Without Jumper to Clear Password
	Pin 5-6	With Jumper to Clear CMOS
DB1	PD 1K	PD 1K to GND for Debug, All Power-On

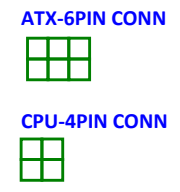
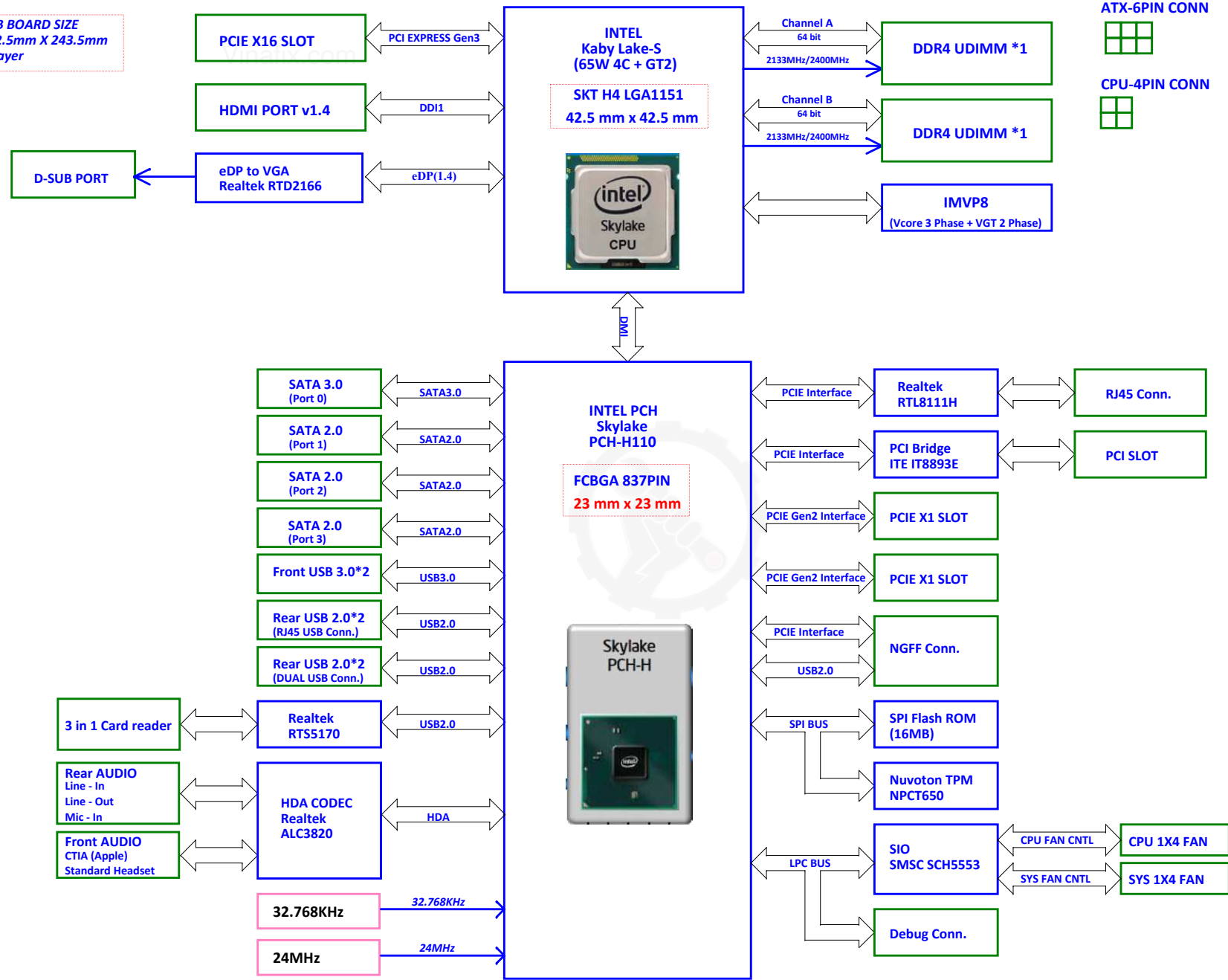
### BOM Configuration

(R\_): Unmount  
(X\_): Debug  
(A\_): Tahoe MT MLK  
(B\_): Tahoe CBB MT MLK  
(T\_): With TPM  
(O\_): Without TPM

### Power sates

	Name	G3	DSW	S5	S4	S3	S0
+12V	V_12P0_A		O	O	O	O	O
	+12V						O
	V_12V_CPU_S0		O	O	O	O	O
-12V	-12V						O
	5V_S0						O
+5V	USBVCC12						
	USBVCC34			O	O	O	O
	USBVCC78						
	5V_S5						
	V_5_CODEC		O	O	O	O	O
	3P3V_S0						O
	3P3V_AUD_S0						
3.3V	3P3V_SB						
	3P3V_SPI						
	3P3V_LAN			O	O	O	O
	3P3V_M2VAUX						
	3P3V_PCIVAUX						
	3P3V_S5		O	O	O	O	O
VBAT	3P0V_BAT_VREG						
	VBAT1	O	O	O	O	O	O
	VBAT2						
VDDQ	+VCCPLL_OC						O
	V_SM					O	O
DIMM	V_SM_VTT						O
	V_VPP						
PCH	V1P0_PCH_SB						
	+V1P0A_VCCAPLL						
	+V1P0A_VCCF24_1P0						
	+V1P0A_VCCAMPHYPLL			O	O	O	O
	V_CPU_ST_PLL						
CPU	V_CPU_CORE						
	V_CPU_GT						
	V_CPU_IO						O
	V_CPU_SA						
	+VCCFUSEPRG						

PCB BOARD SIZE  
282.5mm X 243.5mm  
4 Layer



## DDR DATA

- (11) M\_DATA\_A0\_B3  
(13) M\_DATA\_B0\_B6  
(11) M\_DQS\_A\_DP0\_7  
(11) M\_DQS\_A\_DN0\_7  
(13) M\_DQS\_B\_DP0\_7  
(13) M\_DQS\_B\_DN0\_7

## DDR CMD/ADD

- (11) M\_MAA\_A0\_16  
(11) M\_MAA\_B0\_16  
(11) M\_BA\_A\_0  
(11) M\_BA\_A\_1  
(11) M\_BG\_A\_0  
(11) M\_BG\_A\_1  
(13) M\_BA\_B\_0  
(13) M\_BA\_B\_1  
(13) M\_BG\_B\_0  
(13) M\_BG\_B\_1

## DDR CTRL

- (11) M\_SCS\_A\_N0  
(11) M\_SCS\_A\_N1

- (11) M\_SKE\_A0  
(11) M\_SKE\_A1

- (11) M\_ODT\_A0  
(11) M\_ODT\_A1

- (13) M\_SCS\_B\_N0  
(13) M\_SCS\_B\_N1

- (13) M\_SKE\_B0  
(13) M\_SKE\_B1

- (13) M\_ODT\_B0  
(13) M\_ODT\_B1

## DDR CLOCK

- (11) CK\_M\_DDR0\_A\_DP  
(11) CK\_M\_DDR0\_B\_DN  
(11) CK\_M\_DDR1\_A\_DP  
(11) CK\_M\_DDR1\_B\_DN

- (13) CK\_M\_DDR0\_B\_DP  
(13) CK\_M\_DDR0\_B\_DN  
(13) CK\_M\_DDR1\_B\_DP  
(13) CK\_M\_DDR1\_B\_DN

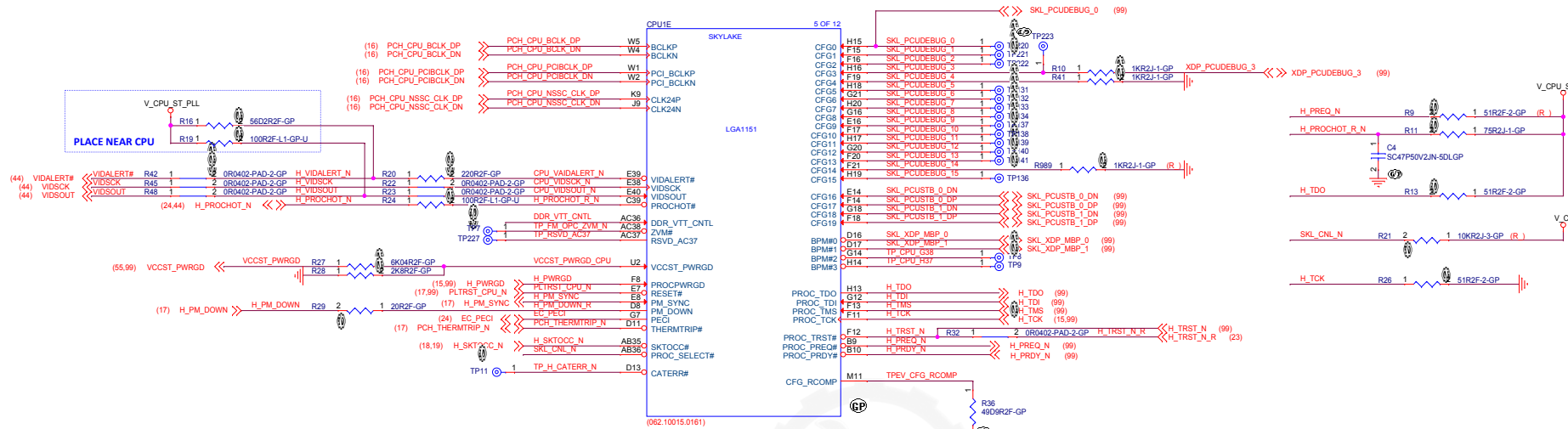
## DDR OTHERS

- (11) DIMM\_CA\_CPU\_VREF\_A  
(13) DIMM\_DQ\_CPU\_VREF\_B

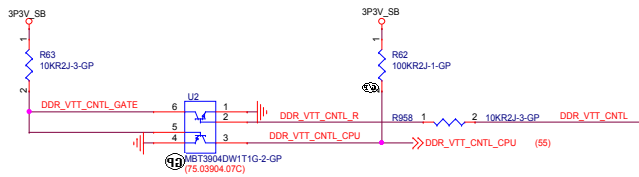
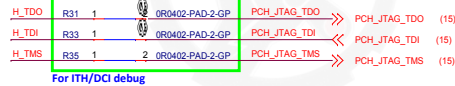
- (11) M\_ACT\_A\_N  
(11) M\_PARITY\_A  
(11) M\_ALERT\_A\_N

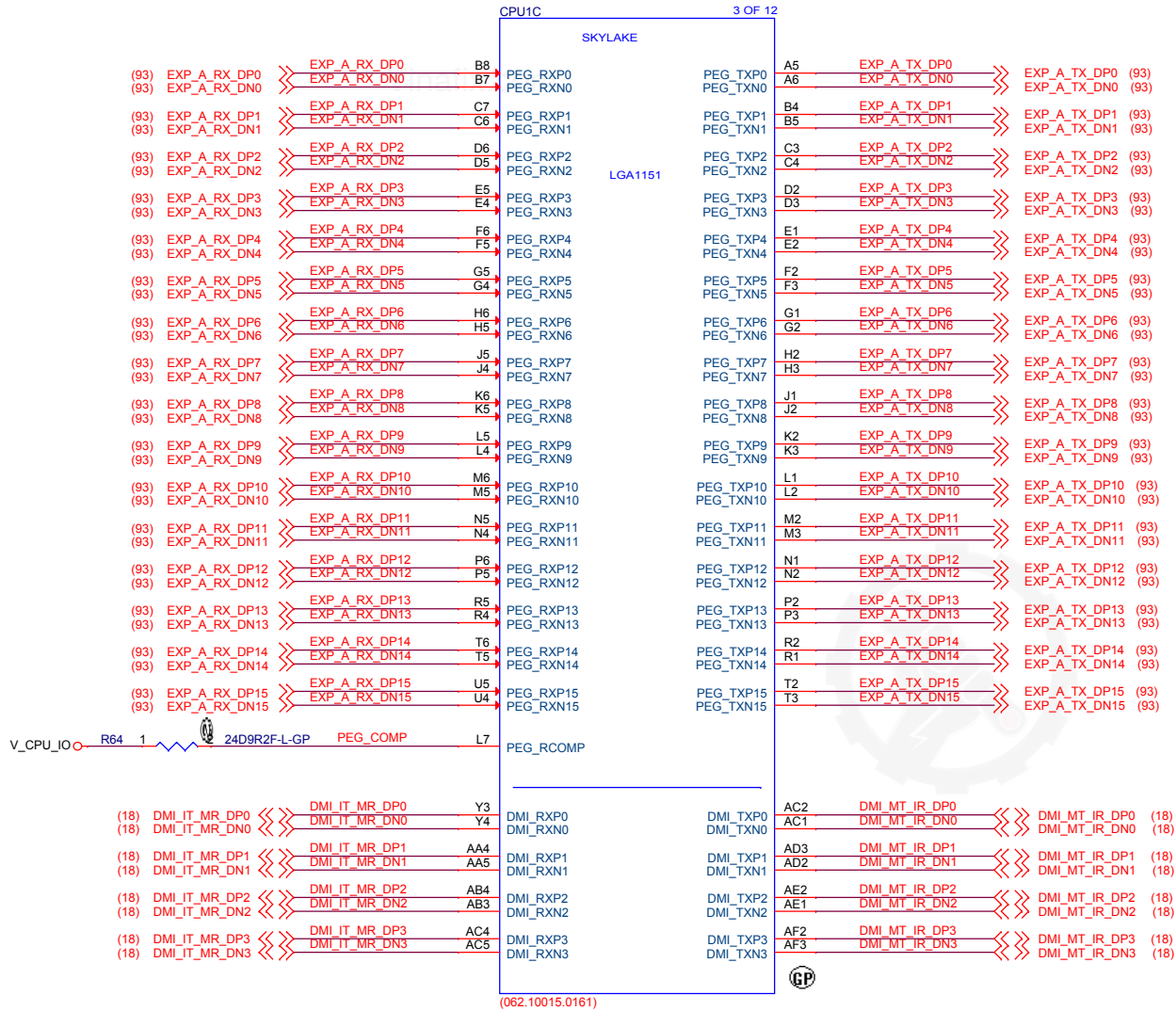
- (13) M\_ACT\_B\_N  
(13) M\_PARITY\_B  
(13) M\_ALERT\_B\_N

CPU1A			SKYLAKE		1 OF 12		
M_DATA_A5	AE38	DDR0_DQ0	DDR0_CK0P	AW18	CK_M_DDR0_A_DP		
M_DATA_A1	AE37	DDR0_DQ1	DDR0_CK0N	AW18	CK_M_DDR0_A_DN		
M_DATA_A2	AE38	DDR0_DQ2	DDR0_CK1P	AW17	CK_M_DDR1_A_DP		
M_DATA_A4	AE39	DDR0_DQ3	DDR0_CK1N	AW18	CK_M_DDR1_A_DN		
M_DATA_A0	AE40	DDR0_DQ4	DDR0_CK2P	AW18			
M_DATA_A6	AE40	DDR0_DQ5	DDR0_CK2N	AW18			
M_DATA_A7	AE40	DDR0_DQ6	DDR0_CK3P	AW18			
M_DATA_A13	AE38	DDR0_DQ7	DDR0_CK3N	AW18			
M_DATA_A9	AE37	DDR0_DQ8		AV24	M_SKE_A0		
M_DATA_A10	AE38	DDR0_DQ9	DDR0_CKE0	AV24	M_SKE_A1		
M_DATA_A11	AE37	DDR0_DQ10	DDR0_CKE1	AV24			
M_DATA_A6	AE40	DDR0_DQ11	DDR0_CKE2	AV24			
M_DATA_A12	AE39	DDR0_DQ12	DDR0_CKE3	AV25			
M_DATA_A14	AE39	DDR0_DQ13					
M_DATA_A15	AE40	DDR0_DQ14	DDR0_CS0	AW18	M_SCS_A_N0		
M_DATA_A21	AN38	DDR0_DQ15	DDR0_CS1	AW18	M_SCS_A_N1		
M_DATA_A16	AN40	DDR0_DQ16	DDR0_CS2	AW18			
M_DATA_A17	AN39	DDR0_DQ17	DDR0_CS3	AW18			
M_DATA_A18	AN38	DDR0_DQ18					
M_DATA_A19	AR37	DDR0_DQ19	DDR0_QD0	AW11	M_ODT_A0		
M_DATA_A20	AN39	DDR0_DQ20	DDR0_QD1	AW14	M_ODT_A1		
M_DATA_A17	AN37	DDR0_DQ21	DDR0_QD2	AW12			
M_DATA_A22	AR39	DDR0_DQ22	DDR0_QD3	AW18			
M_DATA_A23	AR40	DDR0_DQ23	DDR0_QD4				
M_DATA_A24	AN37	DDR0_DQ24	DDR0_QD5	AV13	M_BA_A_0		
M_DATA_A25	AE38	DDR0_DQ25	DDR0_QD6	AV15	M_BA_A_1		
M_DATA_A26	AE38	DDR0_DQ26	DDR0_QD7	AV23	M_BG_A_0		
M_DATA_A27	AE35	DDR0_DQ27	DDR0_QD8	AV13	M_MAA_A16		
M_DATA_A28	AE35	DDR0_DQ28	DDR0_QD9	AV14	M_MAA_A14		
M_DATA_A29	AE35	DDR0_DQ29	DDR0_QD10	AV14	M_MAA_A15		
M_DATA_A30	AE35	DDR0_DQ30	DDR0_QD11	AV15	M_MAA_A16		
M_DATA_A31	AE35	DDR0_DQ31	DDR0_QD12	AV15	M_MAA_A17		
M_DATA_A32	AE35	DDR0_DQ32	DDR0_QD13	AV15	M_MAA_A18		
M_DATA_A33	AE35	DDR0_DQ33	DDR0_QD14	AV15	M_MAA_A19		
M_DATA_A34	AE35	DDR0_DQ34	DDR0_QD15	AV15	M_MAA_A20		
M_DATA_A35	AE35	DDR0_DQ35	DDR0_QD16	AV15	M_MAA_A21		
M_DATA_A36	AE35	DDR0_DQ36	DDR0_QD17	AV15	M_MAA_A22		
M_DATA_A37	AE35	DDR0_DQ37	DDR0_QD18	AV15	M_MAA_A23		
M_DATA_A38	AE35	DDR0_DQ38	DDR0_QD19	AV15	M_MAA_A24		
M_DATA_A39	AE35	DDR0_DQ39	DDR0_QD20	AV15	M_MAA_A25		
M_DATA_A40	AE35	DDR0_DQ40	DDR0_QD21	AV15	M_MAA_A26		
M_DATA_A41	AE35	DDR0_DQ41	DDR0_QD22	AV15	M_MAA_A27		
M_DATA_A42	AE35	DDR0_DQ42	DDR0_QD23	AV15	M_MAA_A28		
M_DATA_A43	AE35	DDR0_DQ43	DDR0_QD24	AV15	M_MAA_A29		
M_DATA_A44	AE35	DDR0_DQ44	DDR0_QD25	AV15	M_MAA_A30		
M_DATA_A45	AE35	DDR0_DQ45	DDR0_QD26	AV15	M_MAA_A31		
M_DATA_A46	AE35	DDR0_DQ46	DDR0_QD27	AV15	M_MAA_A32		
M_DATA_A47	AE35	DDR0_DQ47	DDR0_QD28	AV15	M_MAA_A33		
M_DATA_A48	AE35	DDR0_DQ48	DDR0_QD29	AV15	M_MAA_A34		
M_DATA_A49	AE35	DDR0_DQ49	DDR0_QD30	AV15	M_MAA_A35		
M_DATA_A50	AE35	DDR0_DQ50	DDR0_QD31	AV15	M_MAA_A36		
M_DATA_A51	AE35	DDR0_DQ51	DDR0_QD32	AV15	M_MAA_A37		
M_DATA_A52	AE35	DDR0_DQ52	DDR0_QD33	AV15	M_MAA_A38		
M_DATA_A53	AE35	DDR0_DQ53	DDR0_QD34	AV15	M_MAA_A39		
M_DATA_A54	AE35	DDR0_DQ54	DDR0_QD35	AV15	M_MAA_A40		
M_DATA_A55	AE35	DDR0_DQ55	DDR0_QD36	AV15	M_MAA_A41		
M_DATA_A56	AE35	DDR0_DQ56	DDR0_QD37	AV15	M_MAA_A42		
M_DATA_A57	AE35	DDR0_DQ57	DDR0_QD38	AV15	M_MAA_A43		
M_DATA_A58	AE35	DDR0_DQ58	DDR0_QD39	AV15	M_MAA_A44		
M_DATA_A59	AE35	DDR0_DQ59	DDR0_QD40	AV15	M_MAA_A45		
M_DATA_A60	AE35	DDR0_DQ60	DDR0_QD41	AV15	M_MAA_A46		
M_DATA_A61	AE35	DDR0_DQ61	DDR0_QD42	AV15	M_MAA_A47		
M_DATA_A62	AE35	DDR0_DQ62	DDR0_QD43	AV15	M_MAA_A48		
M_DATA_A63	AE35	DDR0_DQ63	DDR0_QD44	AV15	M_MAA_A49		
M_DATA_A64	AE35	DDR0_DQ64	DDR0_QD45	AV15	M_MAA_A50		
M_DATA_A65	AE35	DDR0_DQ65	DDR0_QD46	AV15	M_MAA_A51		
M_DATA_A66	AE35	DDR0_DQ66	DDR0_QD47	AV15	M_MAA_A52		
M_DATA_A67	AE35	DDR0_DQ67	DDR0_QD48	AV15	M_MAA_A53		
M_DATA_A68	AE35	DDR0_DQ68	DDR0_QD49	AV15	M_MAA_A54		
M_DATA_A69	AE35	DDR0_DQ69	DDR0_QD50	AV15	M_MAA_A55		
M_DATA_A70	AE35	DDR0_DQ70	DDR0_QD51	AV15	M_MAA_A56		
M_DATA_A71	AE35	DDR0_DQ71	DDR0_QD52	AV15	M_MAA_A57		
M_DATA_A72	AE35	DDR0_DQ72	DDR0_QD53	AV15	M_MAA_A58		
M_DATA_A73	AE35	DDR0_DQ73	DDR0_QD54	AV15	M_MAA_A59		
M_DATA_A74	AE35	DDR0_DQ74	DDR0_QD55	AV15	M_MAA_A60		
M_DATA_A75	AE35	DDR0_DQ75	DDR0_QD56	AV15	M_MAA_A61		
M_DATA_A76	AE35	DDR0_DQ76	DDR0_QD57	AV15	M_MAA_A62		
M_DATA_A77	AE35	DDR0_DQ77	DDR0_QD58	AV15	M_MAA_A63		
M_DATA_A78	AE35	DDR0_DQ78	DDR0_QD59	AV15	M_MAA_A64		
M_DATA_A79	AE35	DDR0_DQ79	DDR0_QD60	AV15	M_MAA_A65		
M_DATA_A80	AE35	DDR0_DQ80	DDR0_QD61	AV15	M_MAA_A66		
M_DATA_A81	AE35	DDR0_DQ81	DDR0_QD62	AV15	M_MAA_A67		
M_DATA_A82	AE35	DDR0_DQ82	DDR0_QD63	AV15	M_MAA_A68		
M_DATA_A83	AE35	DDR0_DQ83	DDR0_QD64	AV15	M_MAA_A69		
M_DATA_A84	AE35	DDR0_DQ84	DDR0_QD65	AV15	M_MAA_A70		
M_DATA_A85	AE35	DDR0_DQ85	DDR0_QD66	AV15	M_MAA_A71		
M_DATA_A86	AE35	DDR0_DQ86	DDR0_QD67	AV15	M_MAA_A72		
M_DATA_A87	AE35	DDR0_DQ87	DDR0_QD68	AV15	M_MAA_A73		
M_DATA_A88	AE35	DDR0_DQ88	DDR0_QD69	AV15	M_MAA_A74		
M_DATA_A89	AE35	DDR0_DQ89	DDR0_QD70	AV15	M_MAA_A75		
M_DATA_A90	AE35	DDR0_DQ90	DDR0_QD71	AV15	M_MAA_A76		
M_DATA_A91	AE35	DDR0_DQ91	DDR0_QD72	AV15	M_MAA_A77		
M_DATA_A92	AE35	DDR0_DQ92	DDR0_QD73	AV15	M_MAA_A78		
M_DATA_A93	AE35	DDR0_DQ93	DDR0_QD74	AV15	M_MAA_A79		
M_DATA_A94	AE35	DDR0_DQ94	DDR0_QD75	AV15	M_MAA_A80		
M_DATA_A95	AE35	DDR0_DQ95	DDR0_QD76	AV15	M_MAA_A81		
M_DATA_A96	AE35	DDR0_DQ96	DDR0_QD77	AV15	M_MAA_A82		
M_DATA_A97	AE35	DDR0_DQ97	DDR0_QD78	AV15	M_MAA_A83		
M_DATA_A98	AE35	DDR0_DQ98	DDR0_QD79	AV15	M_MAA_A84		
M_DATA_A99	AE35	DDR0_DQ99	DDR0_QD80	AV15	M_MAA_A85		
M_DATA_A100	AE35	DDR0_DQ100	DDR0_QD81	AV15	M_MAA_A86		
M_DATA_A101	AE35	DDR0_DQ101	DDR0_QD82	AV15	M_MAA_A87		
M_DATA_A102	AE35	DDR0_DQ102	DDR0_QD83	AV15	M_MAA_A88		
M_DATA_A103	AE35	DDR0_DQ103	DDR0_QD84	AV15	M_MAA_A89		
M_DATA_A104	AE35	DDR0_DQ104	DDR0_QD85	AV15	M_MAA_A90		
M_DATA_A105	AE35	DDR0_DQ105	DDR0_QD86	AV15	M_MAA_A91		
M_DATA_A106	AE35	DDR0_DQ106	DDR0_QD87	AV15	M_MAA_A92		
M_DATA_A107	AE35	DDR0_DQ107	DDR0_QD88	AV15	M_MAA_A93		
M_DATA_A108	AE35	DDR0_DQ108	DDR0_QD89	AV15	M_MAA_A94		
M_DATA_A109	AE35	DDR0_DQ109	DDR0_QD90	AV15	M_MAA_A95		
M_DATA_A110	AE35	DDR0_DQ110	DDR0_QD91	AV15	M_MAA_A96		
M_DATA_A111	AE35	DDR0_DQ111	DDR0_QD92	AV15	M_MAA_A97		
M_DATA_A112	AE35	DDR0_DQ112	DDR0_QD93	AV15	M_MAA_A98		
M_DATA_A113	AE35	DDR0_DQ113	DDR0_QD94	AV15	M_MAA_A99		
M_DATA_A114	AE35	DDR0_DQ114	DDR0_QD95	AV15	M_MAA_A100		
M_DATA_A115	AE35	DDR0_DQ115	DDR0_QD96	AV15	M_MAA_A101		
M_DATA_A116	AE35	DDR0_DQ116	DDR0_QD97	AV15	M_MAA_A102		
M_DATA_A117	AE35	DDR0_DQ117	DDR0_QD98	AV15	M_MAA_A103		
M_DATA_A118	AE35	DDR0_DQ118	DDR0_QD99	AV15	M_MAA_A104		
M_DATA_A119	AE35	DDR0_DQ119	DDR0_QD100	AV15	M_MAA_A105		
M_DATA_A120	AE35	DDR0_DQ120	DDR0_QD101	AV15	M_MAA_A106		
M_DATA_A121	AE35	DDR0_DQ121	DDR0_QD102	AV15	M_MAA_A107		
M_DATA_A122	AE35	DDR0_DQ122	DDR0_QD103	AV15	M_MAA_A108		
M_DATA_A123	AE35	DDR0_DQ123	DDR0_QD104	AV15	M_MAA_A109		
M_DATA_A124	AE35	DDR0_DQ124	DDR0_QD105	AV15	M_MAA_A110		
M_DATA_A125	AE35	DDR0_DQ125	DDR0_QD106	AV15	M_MAA_A111		
M_DATA_A126	AE35	DDR0_DQ126	DDR0_QD107	AV15	M_MAA_A112		
M_DATA_A127	AE35	DDR0_DQ127	DDR0_QD108	AV15	M_MAA_A113		
M_DATA_A128	AE35	DDR0_DQ128	DDR0_QD109	AV15	M_MAA_A114		
M_DATA_A129	AE35	DDR0_DQ129	DDR0_QD110	AV15	M_MAA_A115		
M_DATA_A130	AE35	DDR0_DQ130	DDR0_QD111	AV15	M_MAA_A116		
M_DATA_A131	AE35	DDR0_DQ131	DDR0_QD112	AV15	M_MAA_A117		
M_DATA_A132	AE35	DDR0_DQ132	DDR0_QD113	AV15	M_MAA_A118		
M_DATA_A133	AE35	DDR0_DQ133	DDR0_QD114	AV15	M_MAA_A119		
M_DATA_A134	AE35	DDR0_DQ134	DDR0_QD115	AV15	M_MAA_A120		
M_DATA_A135	AE35	DDR0_DQ135	DDR0_QD116	AV15	M_MAA_A121		
M_DATA_A136	AE35	DDR0_DQ136	DDR0_QD117	AV15	M_MAA_A122		
M_DATA_A137	AE35	DDR0_DQ137	DDR0_QD118	AV15	M_MAA_A123		
M_DATA_A138	AE35	DDR0_DQ138	DDR0_QD119	AV15	M_MAA_A124		
M_DATA_A139	AE35	DDR0_DQ139	DDR0_QD120	AV15	M_MAA_A125		
M_DATA_A140	AE35	DDR0_DQ140	DDR0_QD121	AV15	M_MAA_A126		
M_DATA_A141	AE35	DDR0_DQ141	DDR0_QD122	AV15	M_MAA_A127		
M_DATA_A142	AE35	DDR0_DQ142	DDR0_QD123	AV15	M_MAA_A128		
M_DATA_A143	AE35	DDR0_DQ143	DDR0_QD124	AV15	M_MAA_A129		
M_DATA_A144	AE35	DDR0_DQ144	DDR0_QD125	AV15	M_MAA_A130		
M_DATA_A145	AE35	DDR0_DQ145	DDR0_QD126	AV15	M_MAA_A131		
M_DATA_A146	AE35	DDR0_DQ146	DDR0_QD127	AV15	M_MAA_A132		
M_DATA_A147	AE35	DDR0_DQ147	DDR0_QD128	AV15	M_MAA_A133		
M_DATA_A148	AE35	DDR0_DQ148	DDR0_QD129	AV15	M_MAA_A134		
M_DATA_A149	AE35	DDR0_DQ149	DDR0_QD130	AV15	M_MAA_A135		
M_DATA_A150	AE35	DDR0_DQ150	DDR0_QD131	AV15	M_MAA_A136		
M_DATA_A151	AE35	DDR0_DQ151	DDR0_QD132	AV15	M_MAA_A137		
M_DATA_A152	AE35	DDR0_DQ152	DDR0_QD133	AV15	M_MAA_A138		
M_DATA_A153	AE35	DDR0_DQ153	DDR0_QD134	AV15	M_MAA_A139		
M_DATA_A154	AE35	DDR0_DQ154	DDR0_QD135	AV15	M_MAA_A140		
M_DATA_A155	AE35	DDR0_DQ155	DDR0_QD136	AV15	M_MAA_A141		
M_DATA_A156	AE35	DDR0_DQ156	DDR0_QD137	AV15	M_MAA_A142		
M_DATA_A157	AE35	DDR0_DQ157	DDR0_QD138	AV15	M_MAA_A143		
M_DATA_A158	AE35	DDR0_DQ158	DDR0_QD139	AV15	M_MAA_A144		
M_DATA_A159	AE35	DDR0_DQ159	DDR0_QD140	AV15	M_MAA_A145		
M_DATA_A160	AE35	DDR0_DQ160	DDR0_QD141	AV15	M_MAA_A146		
M_DATA_A161	AE35	DDR0_DQ161	DDR0_QD142	AV15	M_MAA_A147		
M_DATA_A162	AE35	DDR0_DQ162	DDR0_QD143	AV15	M_MAA_A148		
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M_DATA_A165	AE35	DDR0_DQ165	DDR0_QD146	AV15	M_MAA_A151		
M_DATA_A166	AE35	DDR0_DQ166	DDR0_QD147	AV15	M_MAA_A152		
M_DATA_A167	AE35	DDR0_DQ167	DDR0_QD148	AV15	M_MAA_A153		
M_DATA_A168	AE35	DDR0_DQ168	DDR0_QD149	AV15	M_MAA_A154		
M_DATA_A169	AE35	DDR0_DQ169	DDR0_QD150	AV15	M_MAA_A155		
M_DATA_A170	AE35	DDR0_DQ170	DDR0_QD151	AV15	M_MAA_A156		
M_DATA_A171	AE35	DDR0_DQ171	DDR0_QD152	AV15	M_MAA_A157		
M_DATA_A172	AE35	DDR0_DQ172	DDR0_QD153	AV15	M_MAA_A158		
M_DATA_A173	AE35	DDR0_DQ173	DDR0_QD154	AV15	M_MAA_A159		
M_DATA_A174	AE35	DDR0_DQ174	DDR0_QD155	AV15	M_MAA_A160		
M_DATA_A175	AE35	DDR0_DQ175	DDR0_QD156	AV15	M_MAA_A161		
M_DATA_A176	AE35	DDR0_DQ176	DDR0_QD157	AV15	M_MAA_A162		
M_DATA_A177	AE35	DDR0_DQ177	DDR0_QD158	AV15	M_MAA_A163		
M_DATA_A178	AE35	DDR0_DQ178	DDR0_QD159	AV15	M_MAA_A164		
M_DATA_A179	AE35	DDR0_DQ179	DDR0_QD160	AV15	M_MAA_A165		
M_DATA_A180	AE35	DDR0_DQ180	DDR0_QD161	AV15	M_MAA_A166		
M_DATA_A181	AE35	DDR0_DQ181	DDR0_QD162	AV15	M_MAA_A167		
M_DATA_A182	AE35	DDR0_DQ182	DDR0_QD163	AV15	M_MAA_A168		
M_DATA_A183	AE35	DDR0_DQ183	DDR0_QD164	AV15	M_MAA_A169		
M_DATA_A184	AE35	DDR0_DQ184	DDR0_QD165	AV15	M_MAA_A170		
M_DATA_A185	AE35	DDR0_DQ185	DDR0_QD166	AV15	M_MAA_A171		
M_DATA_A186	AE35	DDR0_DQ186	DDR0_QD167	AV15	M_MAA_A172		
M_DATA_A187	AE35	DDR0_DQ187					



## For EMI





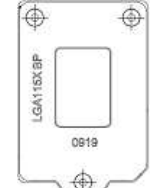
## SKYLAKE SOCKET

SKT1



Load Plate  
(22.78003.021)

SKT2



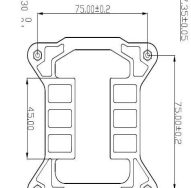
Back Plate  
(22.78006.031)

SKT4



ILMCOVER  
(22.78005.171)

SKT3

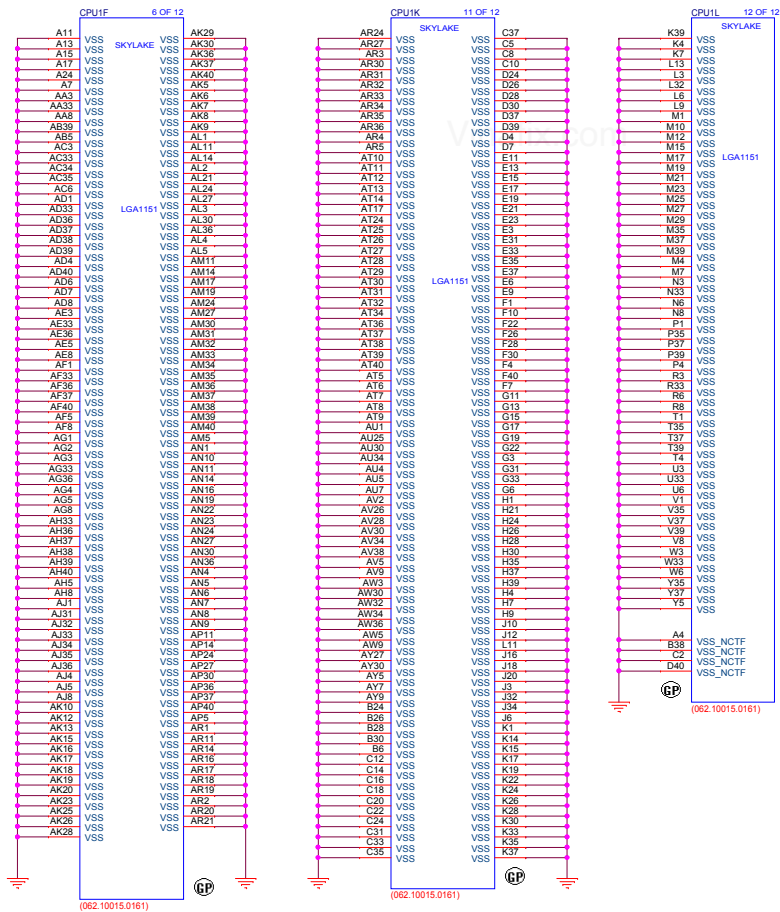


ASSY BACK PLATE  
(60.3EQ19.002)

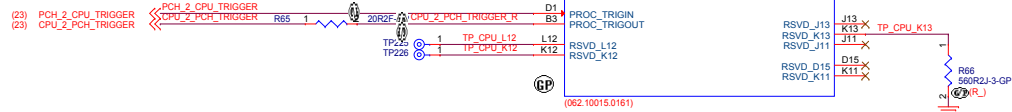


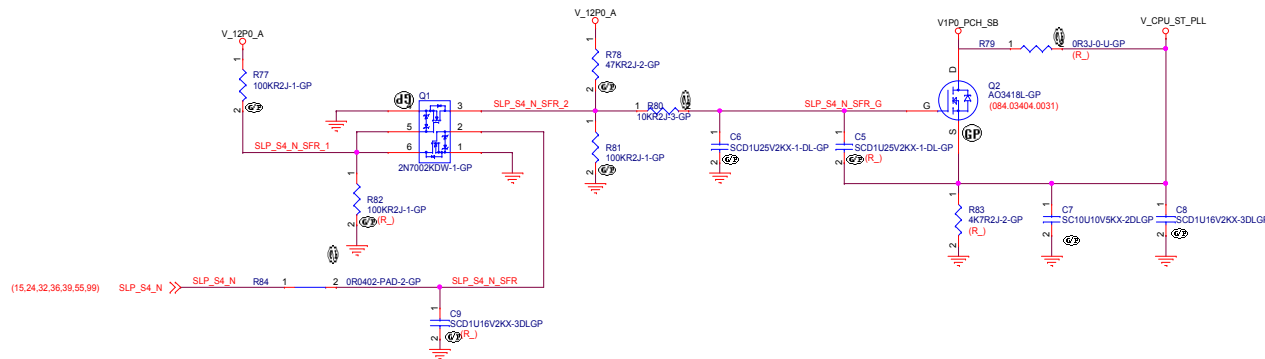
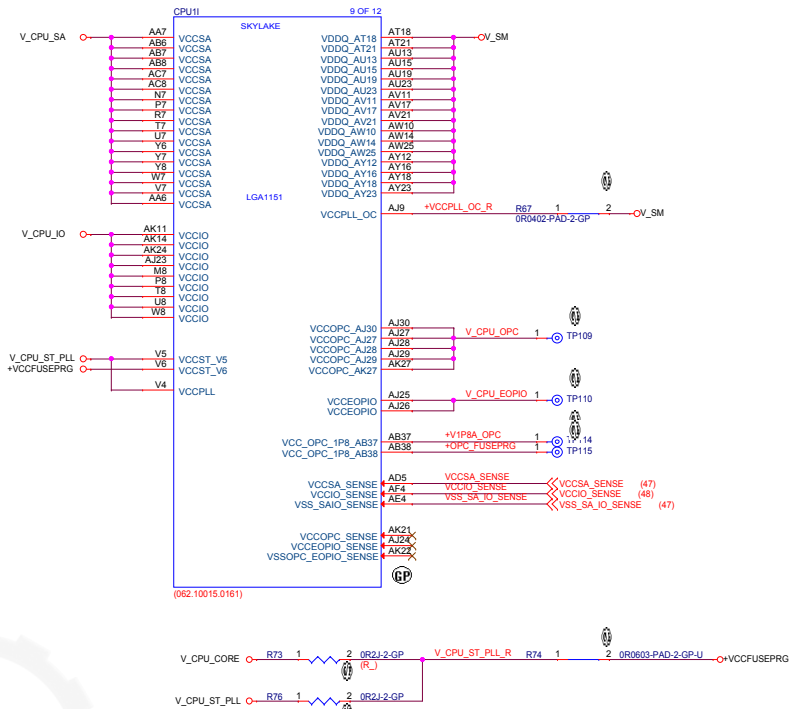
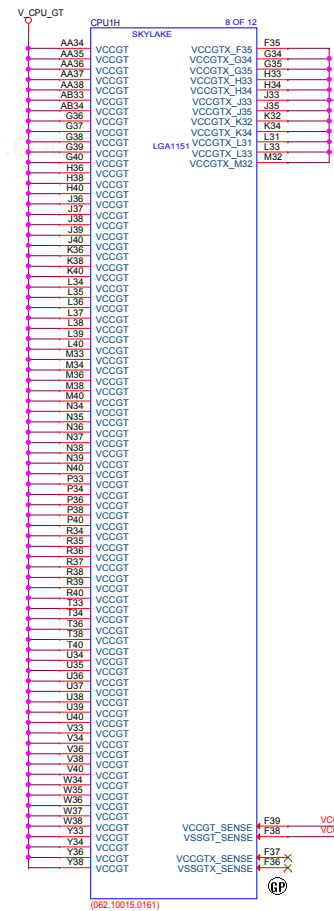
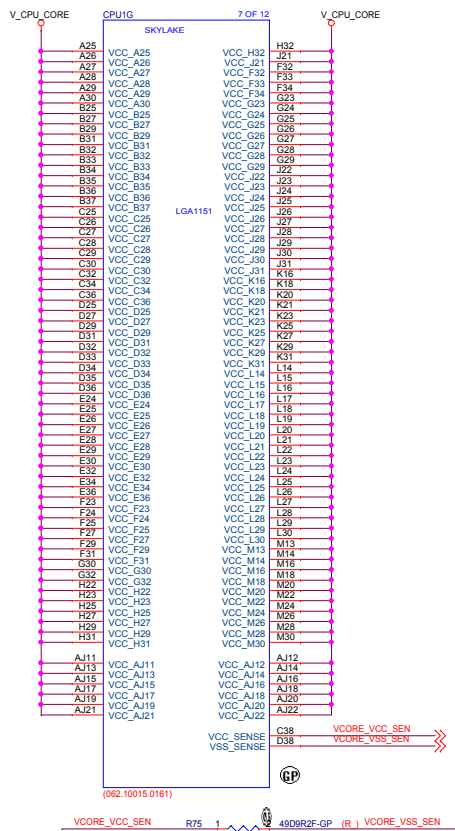
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Taipei Hsien 221, Taiwan, R.O.C.

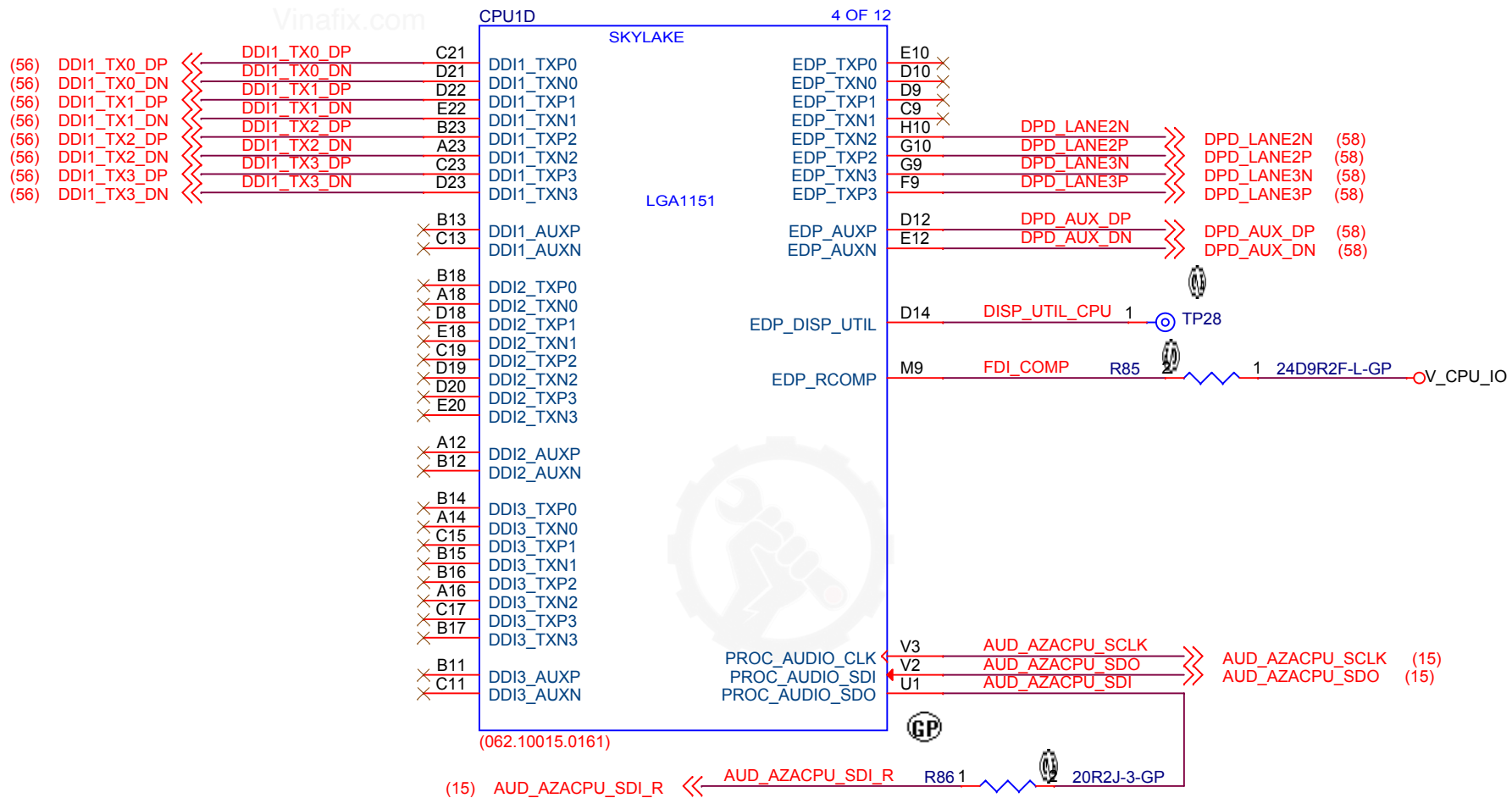
Title <b>CPU_(PCIE)</b>		
Size <b>B</b>	Document Number <b>Tahoe MT MLK/Gambits MT KBL</b>	Rev <b>A00</b>
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(23) PCH\_2\_CPU\_TRIGGER  
(23) CPU\_Z\_PCH\_TRIGGER







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Title

**CPU\_(DDI/EDP)**

Size

**A**

Document Number

**Tahoe MT MLK/Gambits MT KBL**

Rev

**A00**

Date:

Wednesday, October 19, 2016

Sheet

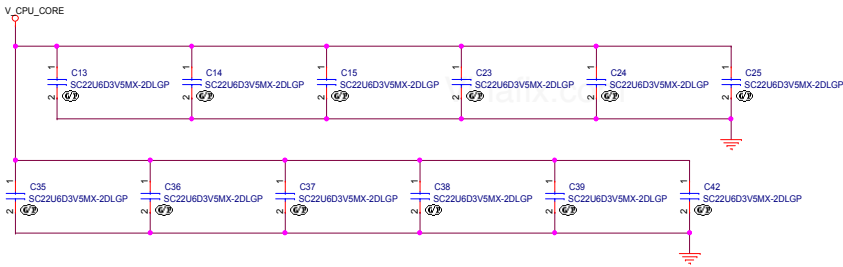
8

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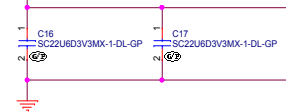
107



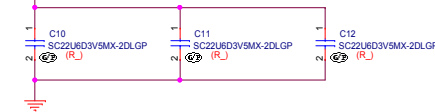
PLACE ALL 0805 CAPS ON TOP SIDE OF CPU CAVITY



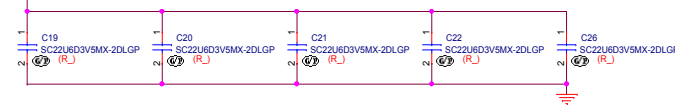
PLACE ALL 0603 CAPS ON TOP SIDE OF CPU CAVITY



IF Have enough TOP SIDE OF CPU CAVITY, On it, Or at socket EDGE

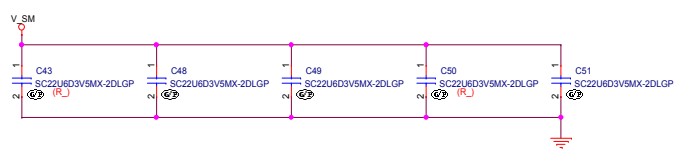


PLACE ALL 0805 CAPS AT TOP SOCKET EDGE

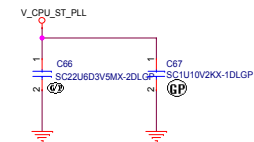


PLACE CAPS FOR DIMM

PLACE CAPS IN SOCKET EDGE TOP



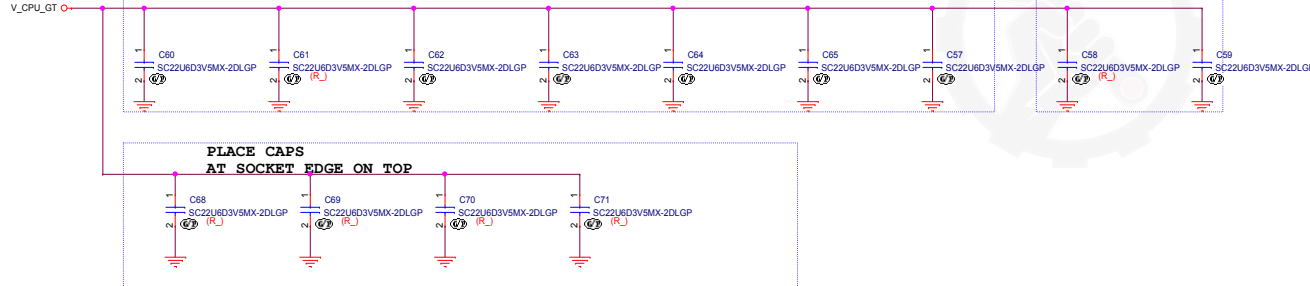
VCCST/VCCSTG  
PLACE CAPS AT TOP SOCKET EDGE



CRB:1\*22U  
0805,1\*1U 0402

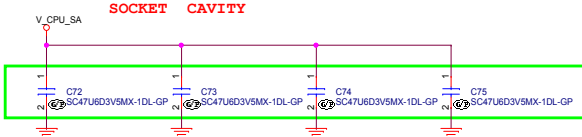
PLACE CAPS ON TOP SIDE  
SOCKET CAVITY

PLACE CAPS  
IN SOCKET EDGE TOP



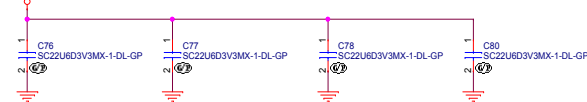
PLACE CAPS ON TOP SIDE  
SOCKET CAVITY

PLACE CAPS AT TOP SOCKET EDGE



CRB:4\*22U 0603

PLACE CAPS ON TOP SIDE  
SOCKET CAVITY



CRB:1\*22U  
0805,5\*22U 0603

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Reserved**

Size

**A**

Document Number

**Tahoe MT MLK/Gambits MT KBL**

Rev

**A00**

Date:

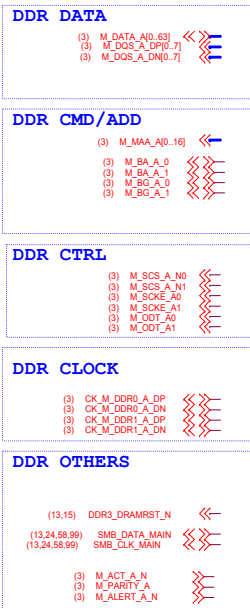
Wednesday, October 19, 2016

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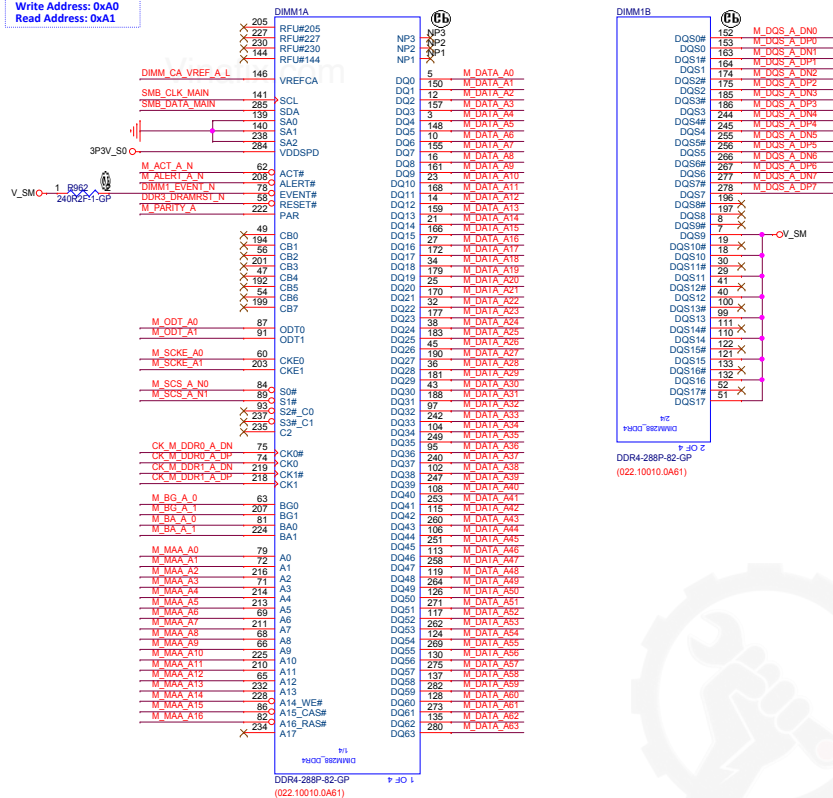
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of

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**DIMM1:**  
SA0: 0, SA1: 0  
Write Address: 0xA0  
Read Address: 0xA1



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Size

**A**

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DDR DATA

(3) M\_DATA\_B0\_63  
(3) M\_DQS\_B\_DP0-7  
(3) M\_QOS\_B\_DP0-7

DDR CMD/ADD

(3) M\_MAA\_B0-16  
(3) M\_BA\_B\_0  
(3) M\_BA\_B\_1  
(3) M\_B0\_B\_0  
(3) M\_B0\_B\_1

DDR CTRL

(3) M\_SCS\_B\_N0  
(3) M\_SCS\_B\_N1  
(3) M\_SCKE\_B0  
(3) M\_SCKE\_B1  
(3) M\_ODT\_B0  
(3) M\_ODT\_B1

DDR CLOCK

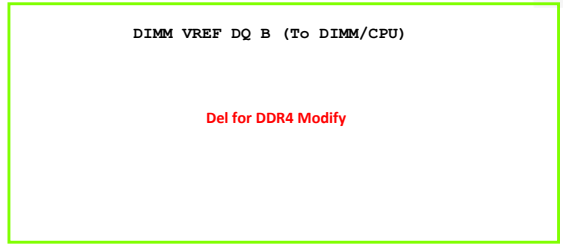
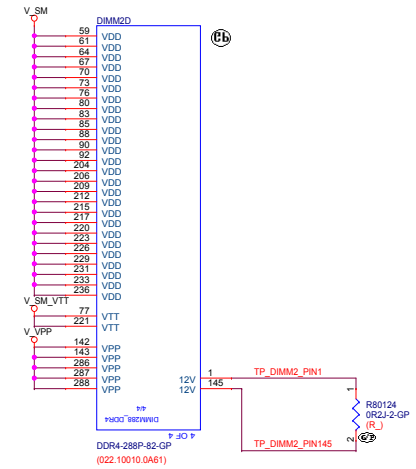
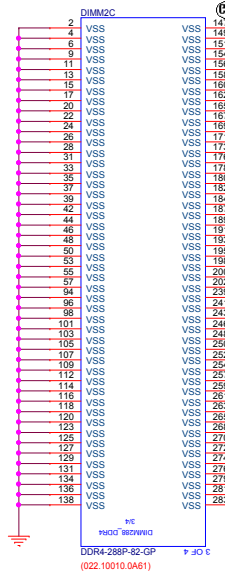
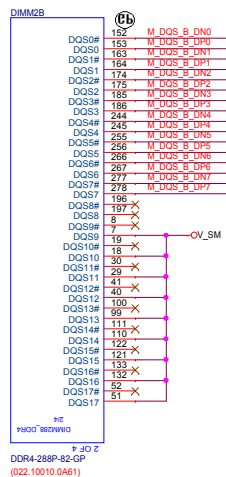
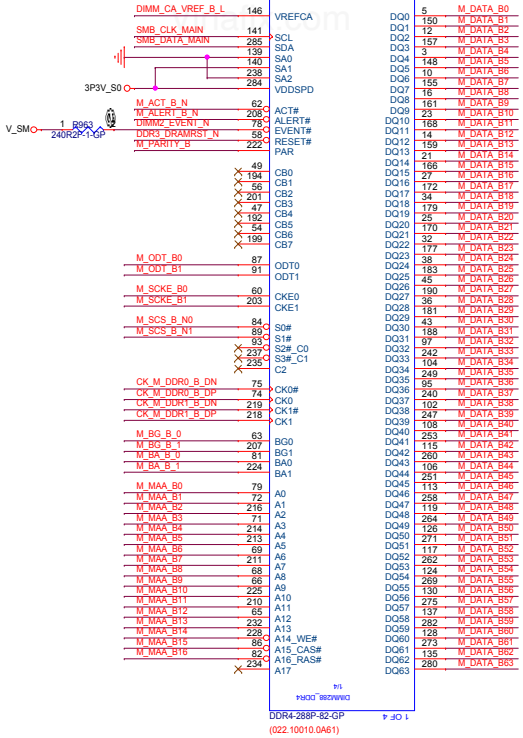
(3) CK\_M\_DDR0\_B\_DP  
(3) CK\_M\_DDR0\_B\_DN  
(3) CK\_M\_DDR1\_B\_DP  
(3) CK\_M\_DDR1\_B\_DN

DDR OTHERS

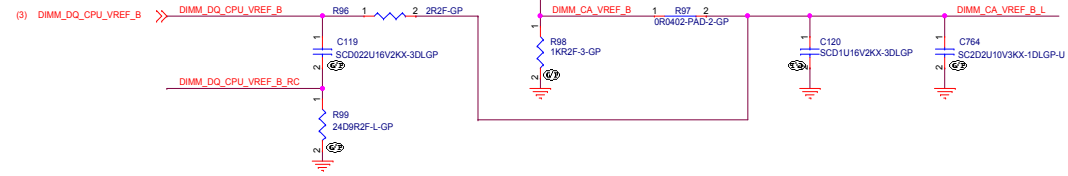
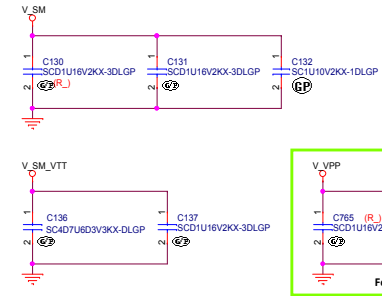
(11,15) DDR3\_DRAMRST\_N  
(11,24,58,99) SMB\_DATA\_MAIN  
(11,24,58,99) SMB\_CLK\_MAIN

(3) M\_ACT\_B\_N  
(3) M\_PARITY\_B  
(3) M\_ALERT\_B\_N

DIMM2:  
SA0: 0, SA1: 1  
Write Address: 0xA5  
Read Address: 0xA5



Del for DDR4 Modify



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Title

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Size

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Document Number

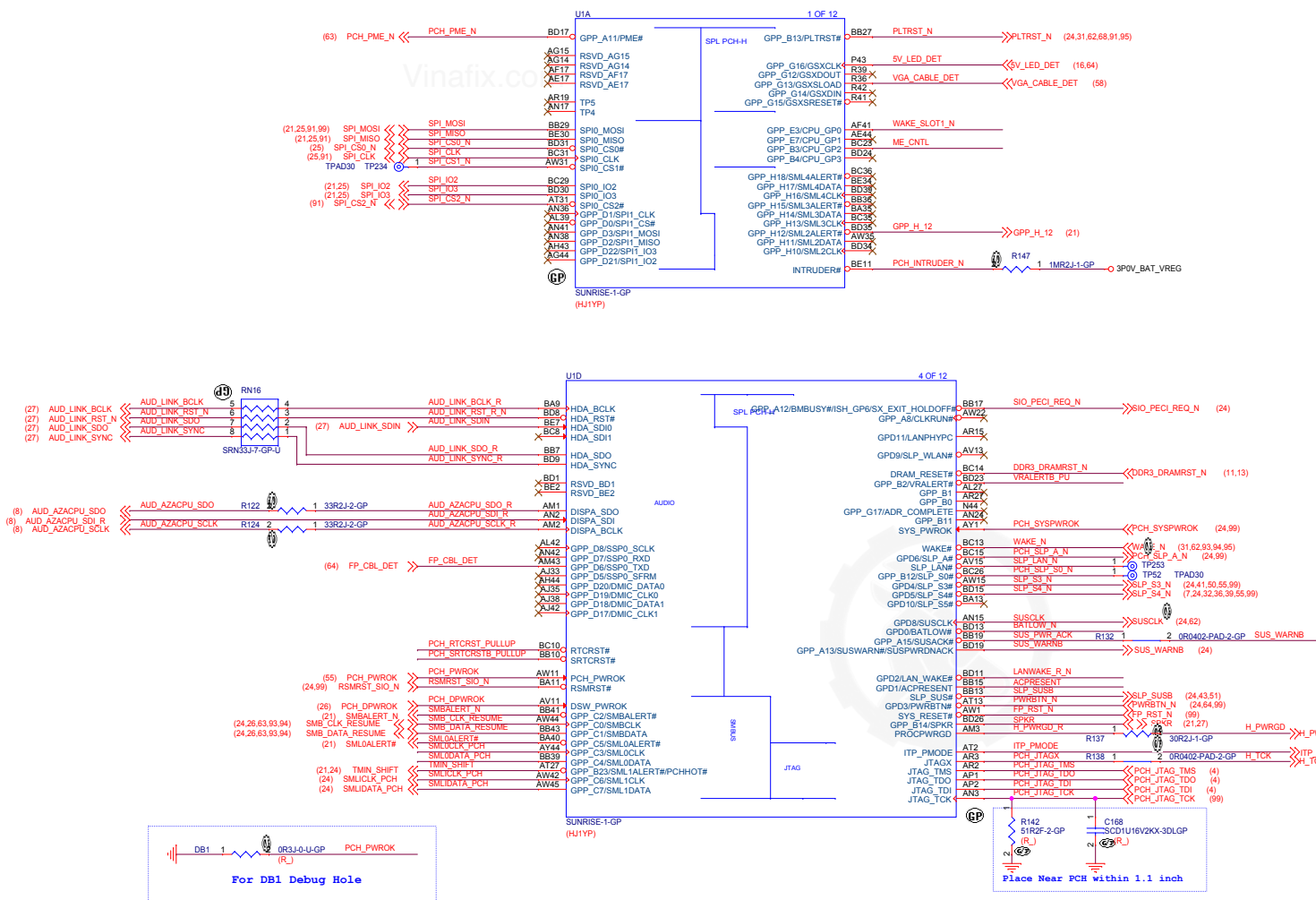
**Tahoe MT MLK/Gambits MT KBL**

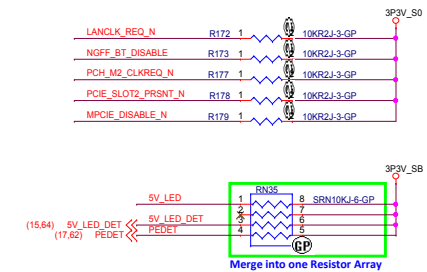
Rev

**A00**

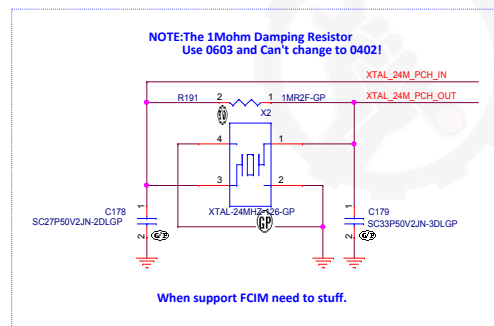
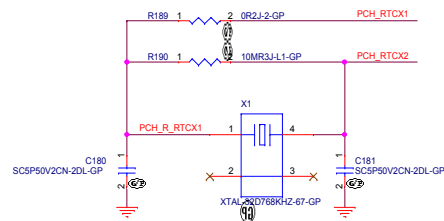
Date: Wednesday, October 19, 2016

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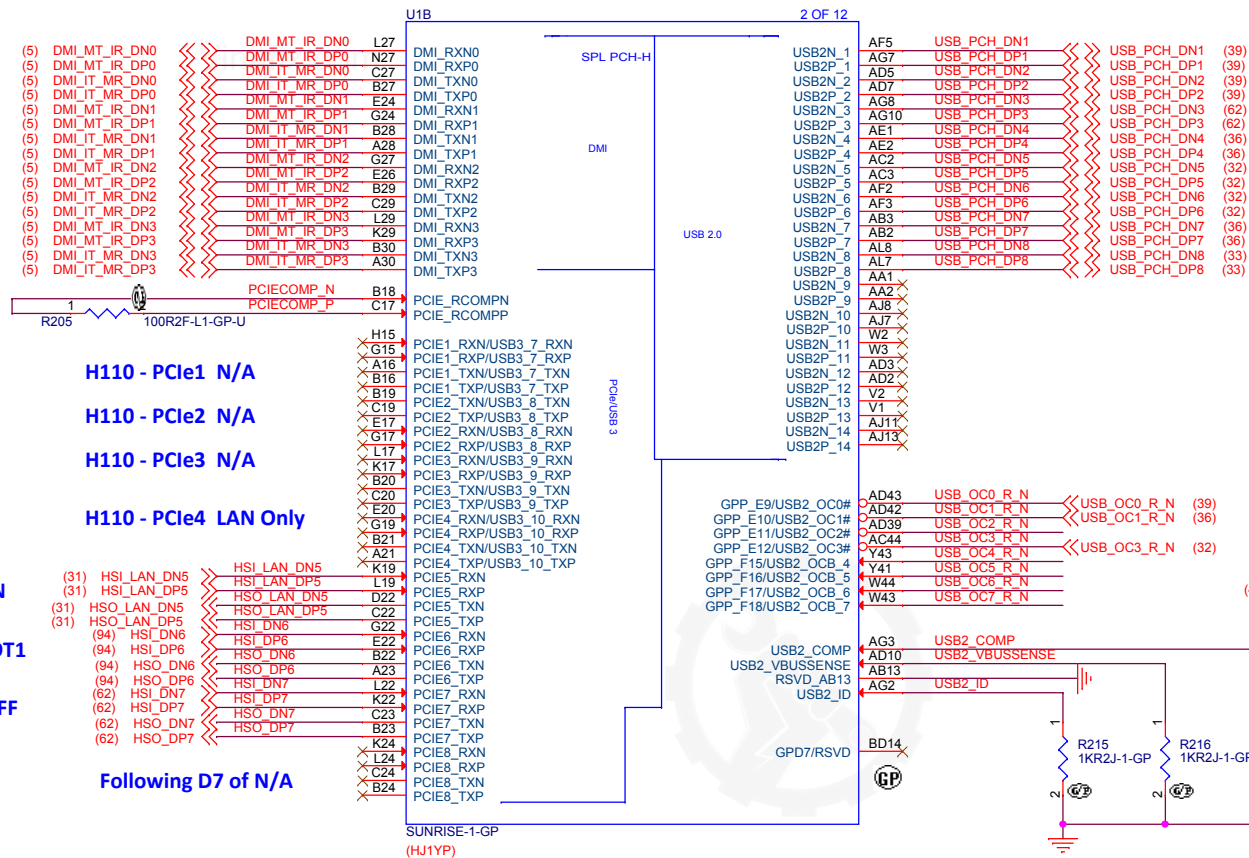
**NOTE: The 1Mohm Damping Resistor  
Use 0603 and Can't change to 0402!**



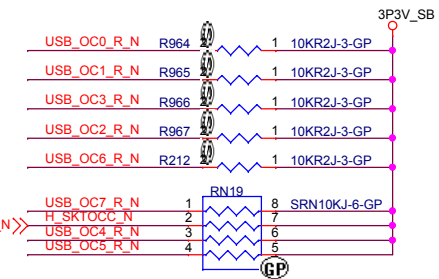
When support FCIM need to stuff.







Front USB 3.0  
Front USB 3.0  
NGFF  
Rear USB 2.0  
RJ45  
RJ45  
Rear USB 2.0  
Card Reader



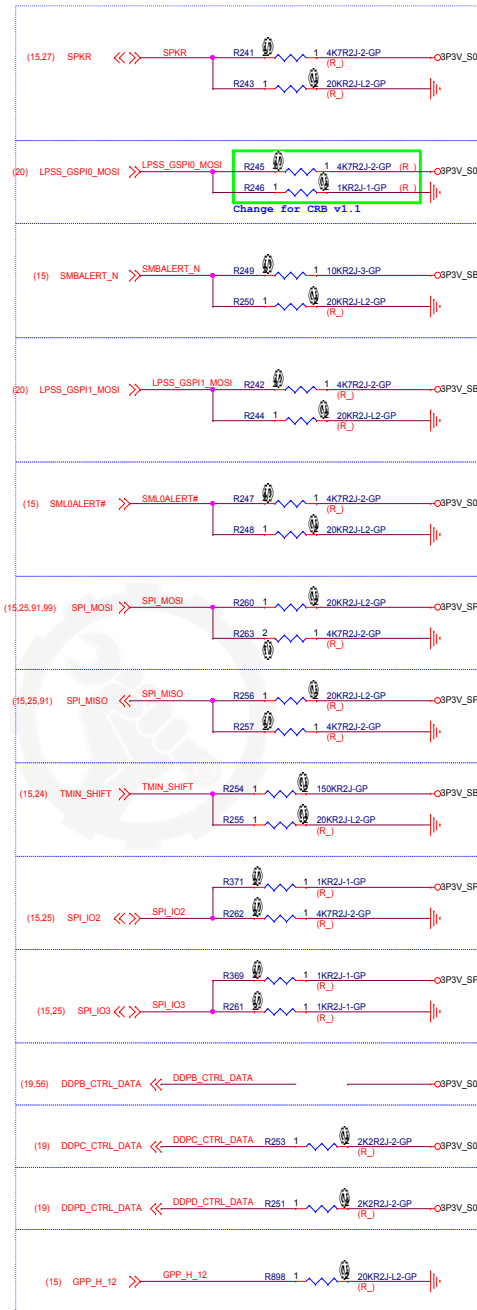
H110 - PCIe1 for LAN  
H110 - PCIe1 for SLOT1  
H110 - PCIe1 for NGFF

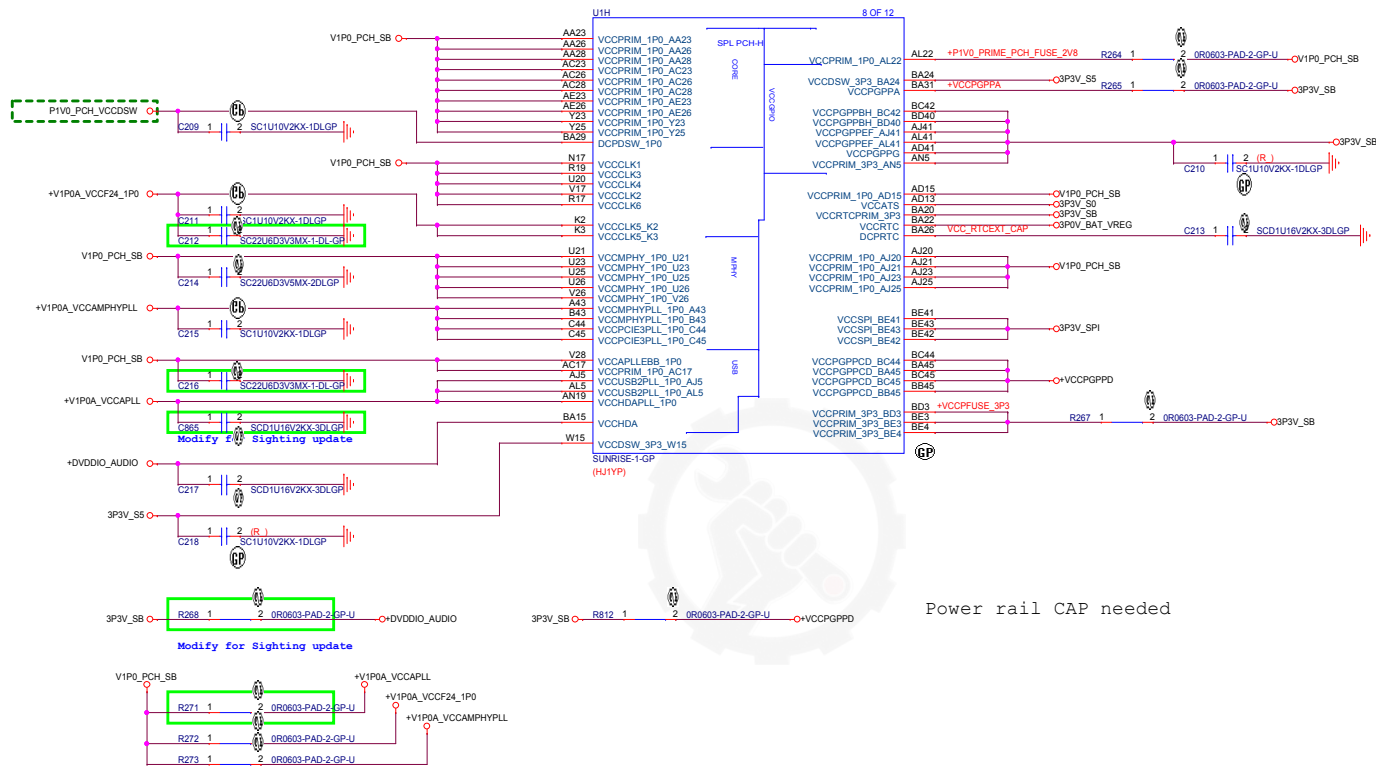
H110 - PCIe1 N/A  
H110 - PCIe2 N/A  
H110 - PCIe3 N/A  
H110 - PCIe4 LAN Only  
Following D7 of N/A



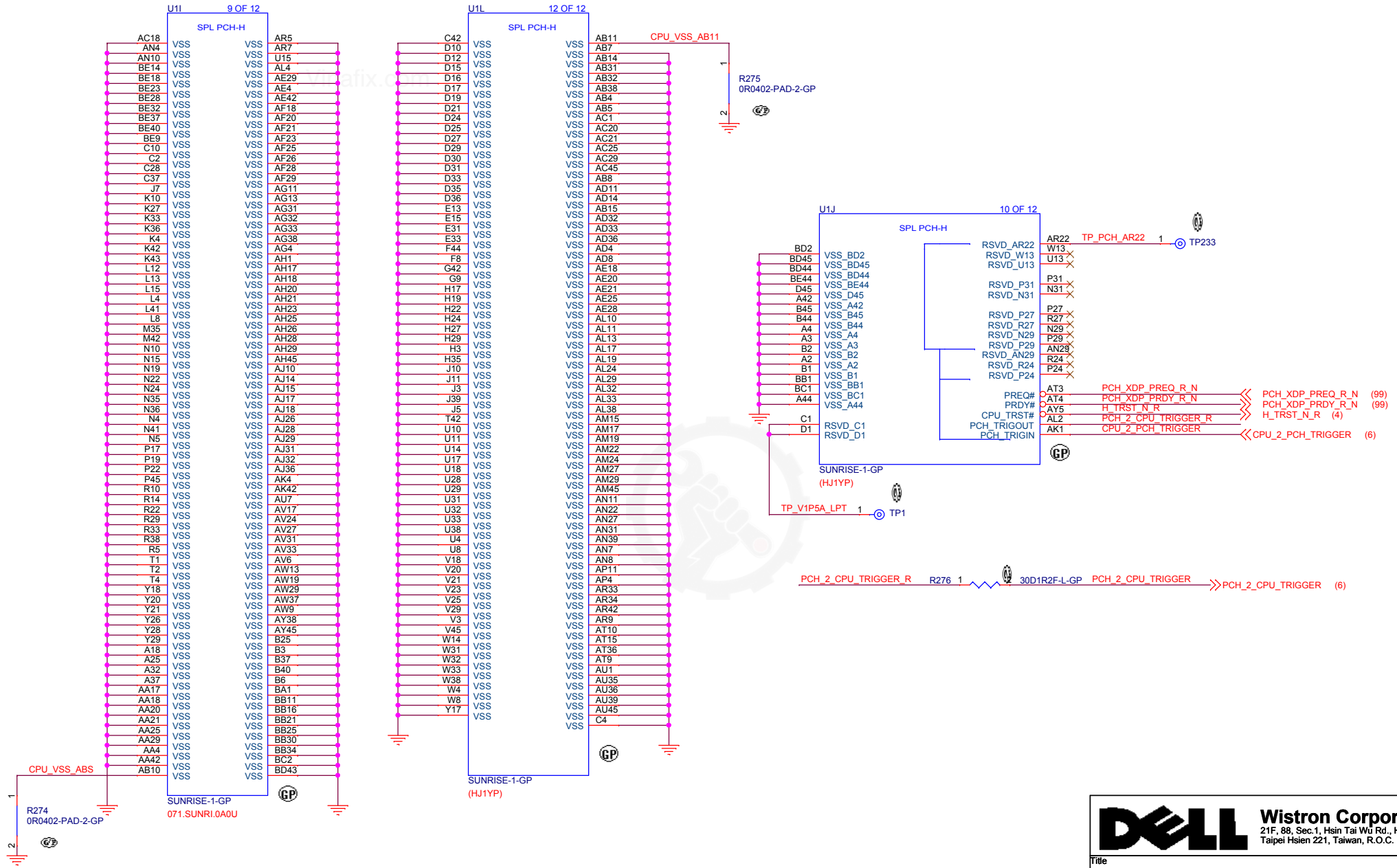



<b>SPKR/GPP_B14</b>	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = Disable "Top Swap" mode. (Default) 1 = Enable "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap
<b>GSPI0_MOSI/GPP_B18</b>	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = Disable "No Reboot" mode. (Default) 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.
<b>SMBALERT#/GPP_C2</b>	TLS Confidentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.
<b>GSPI1_MOSI/GPP_B22</b>	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset BCh, bit 6). Bit 6      Boot BIOS Destination 0          SPI (Default) 1          LPC
<b>SMLALERT#/GPP_C5</b>	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = LPC Is selected for EC. (Default) 1 = eSPI Is selected for EC. Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
<b>SPI0_MOSI</b>	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
<b>SPI0_MISO</b>	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
<b>SMLALERT#/PCHHOT#/GPP_B23</b>	Reserved	Rising edge of RSMRST#	This signal has an internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.
<b>SPI0_IO2</b>	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
<b>SPI0_IO3</b>	Reserved	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
<b>DDPB_CTRLDATA/GPP_I16</b>	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port B is not detected. (Default) 1 = Port B is detected.
<b>DDPC_CTRLDATA/GPP_I16</b>	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected.
<b>DDPD_CTRLDATA/GPP_I10</b>	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected.
<b>GPP_H12</b>	Reserved	Rising edge of RSMRST#	This signal has a weak internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.

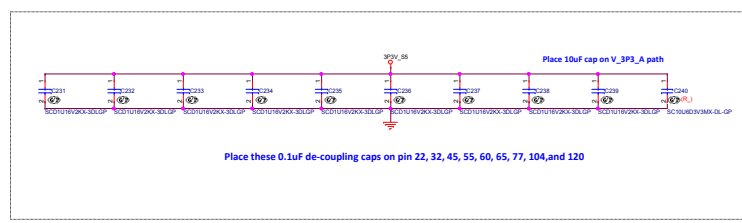
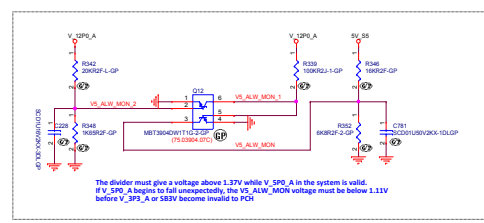
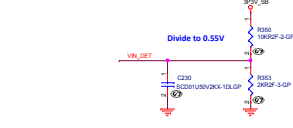
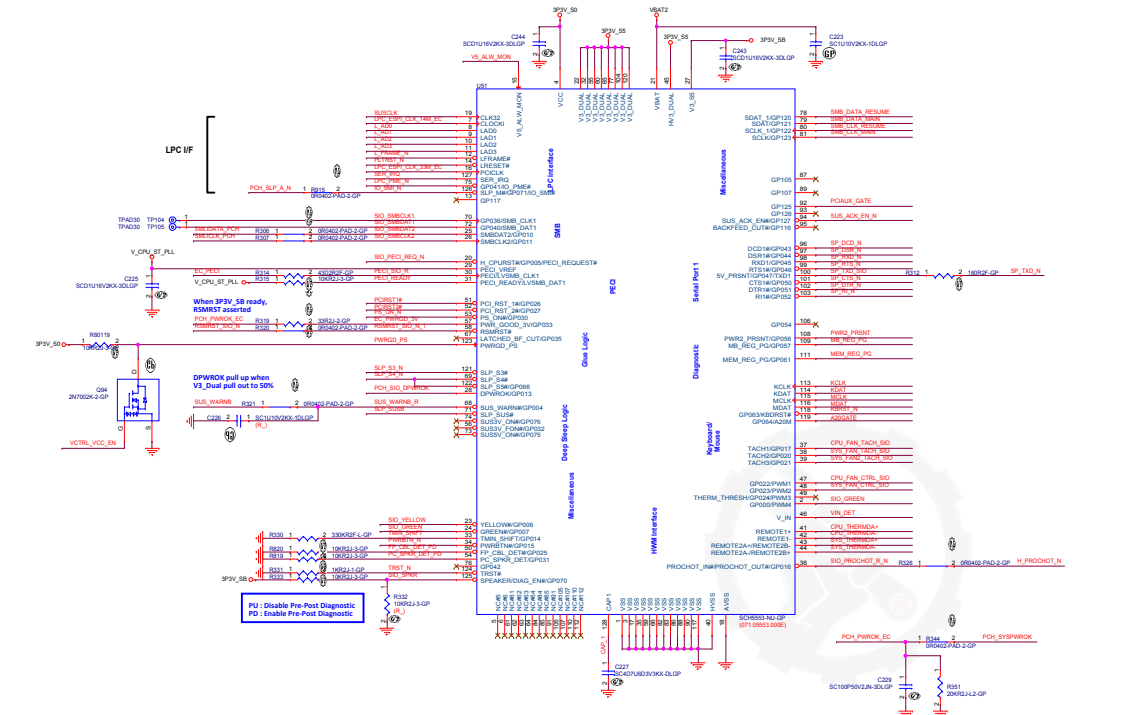
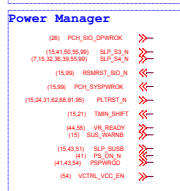
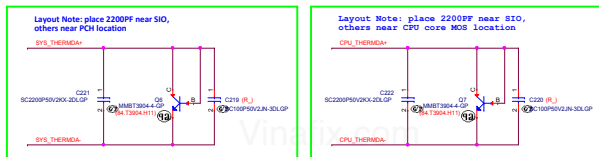




Power rail CAP needed



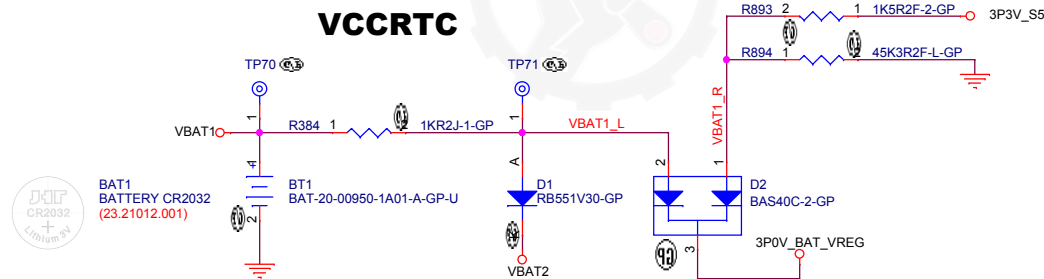
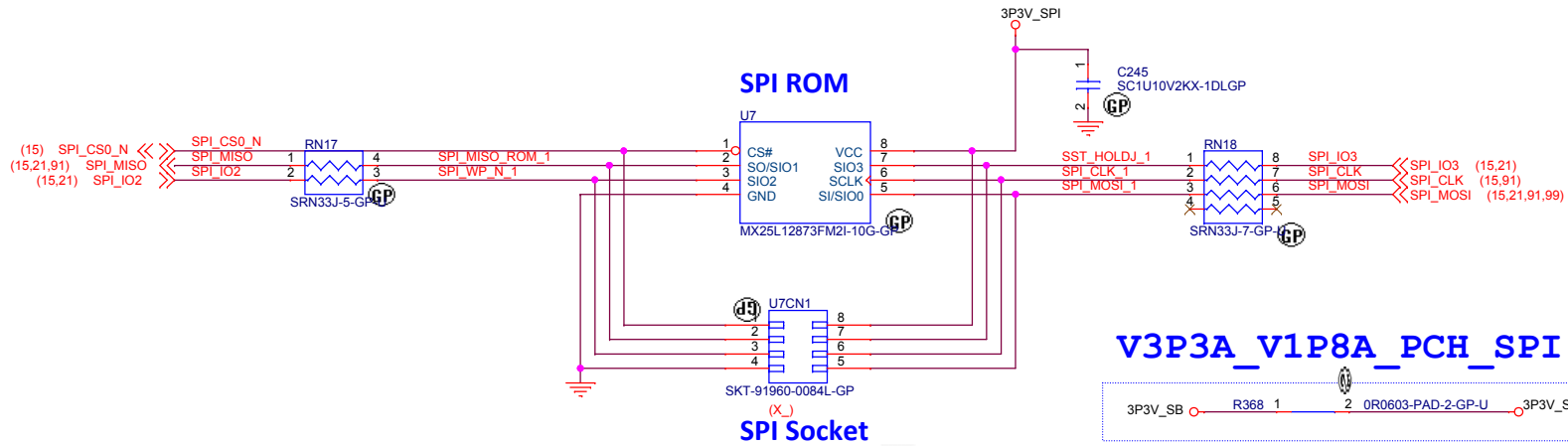
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wuj Rd., Hsieh, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>PCH_(VSS/GPIO)</b>			
Size <b>B</b>	Document Number <b>Tahoe MT MLK/Gambits MT KBL</b>		Rev <b>A00</b>
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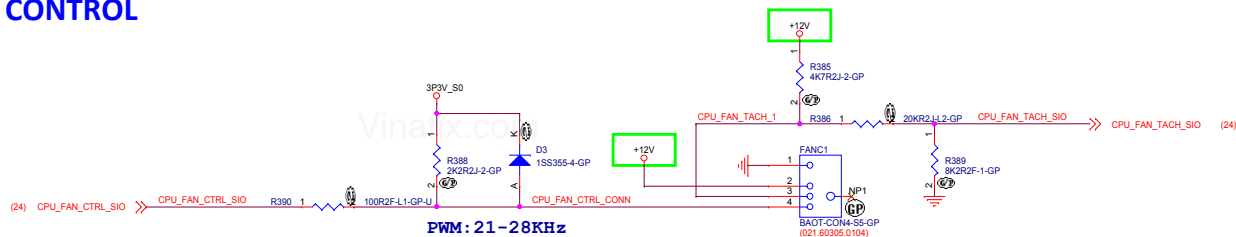
	BC85555(S)	BC85555(T)
Pin 3	GP001	VSS
Pin 5	GP002	NC
Pin 6	GP003	NC
Pin 61	GP111	NC
Pin 62	GP112	NC
Pin 63	GP113	NC
Pin 64	GP114	NC
Pin 82	NC, INT_VS	VSS
Pin 83	NC, INT_VS	VSS
Pin 84	NC, CLK_VS	VSS
Pin 85	NC, CLK_VS	VSS
Pin 86	GP104	VSS
Pin 88	GP105	VSS
Pin 91	EXTAL, CPLE	
Pin 92	EXTAL, CPLE	
Pin 95	EXTAL, CPLE	GP125
Pin 100	GP053	NC
Pin 107	GP055	NC
Pin 110	GP060	NC
Pin 112	GP061	NC



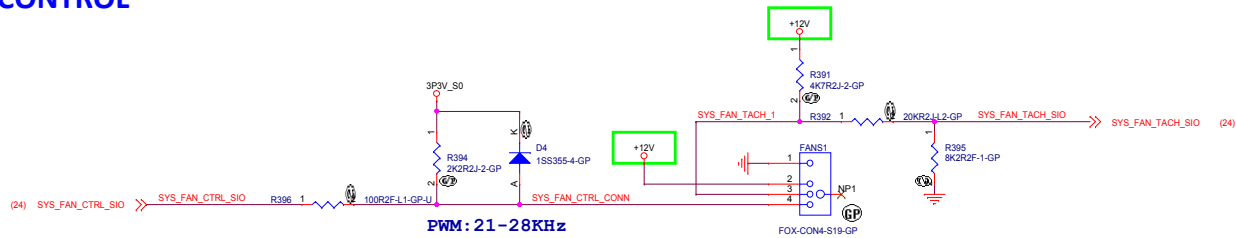
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## CPU FAN CONTROL



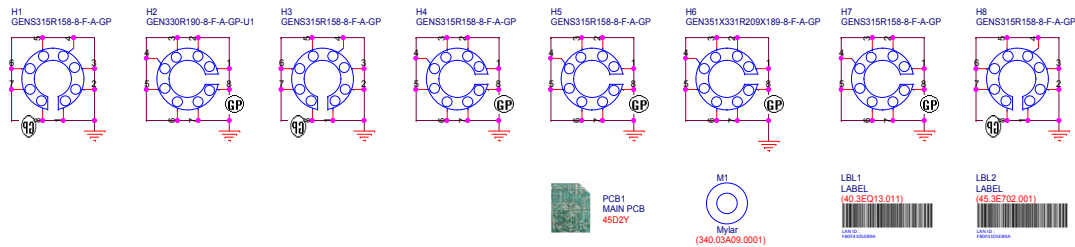
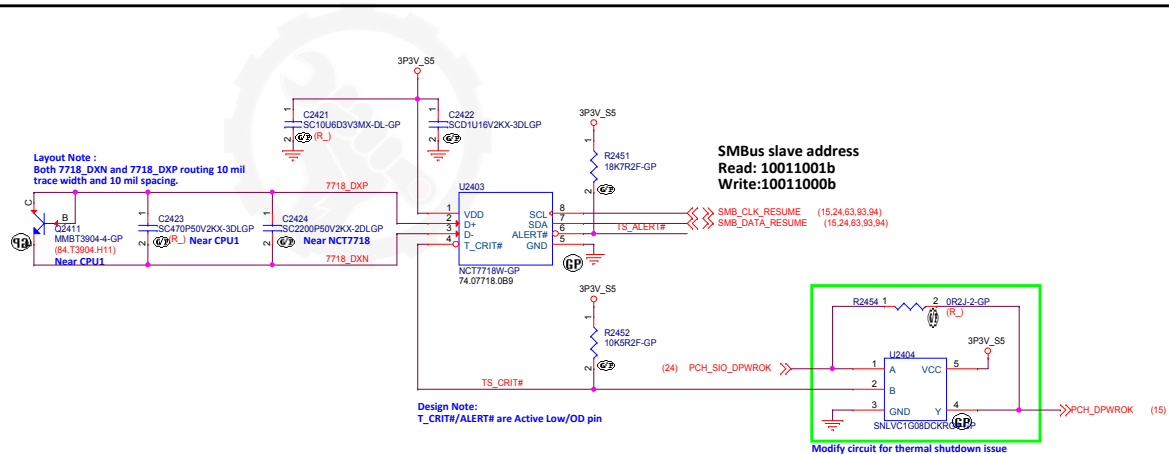
## SYS FAN CONTROL

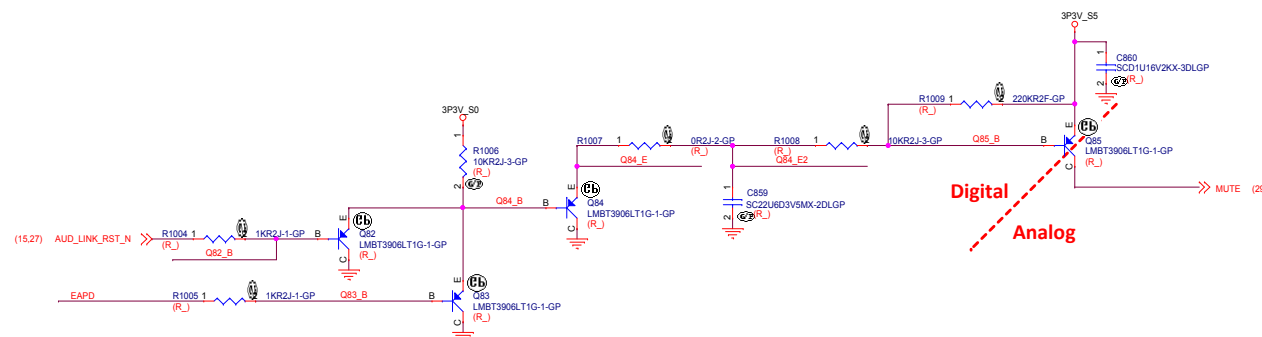
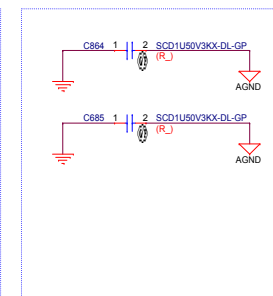
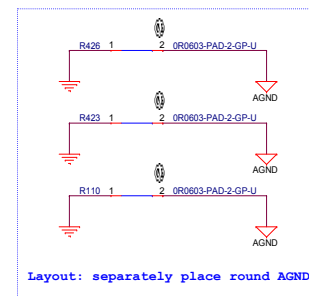
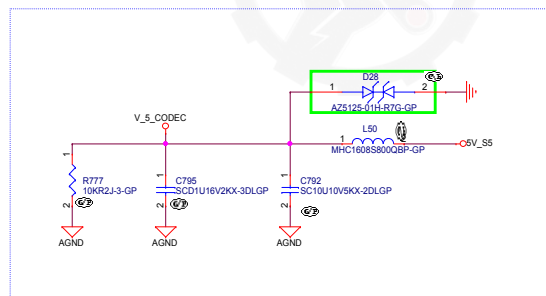
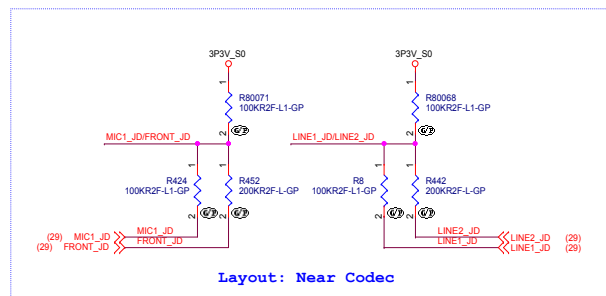
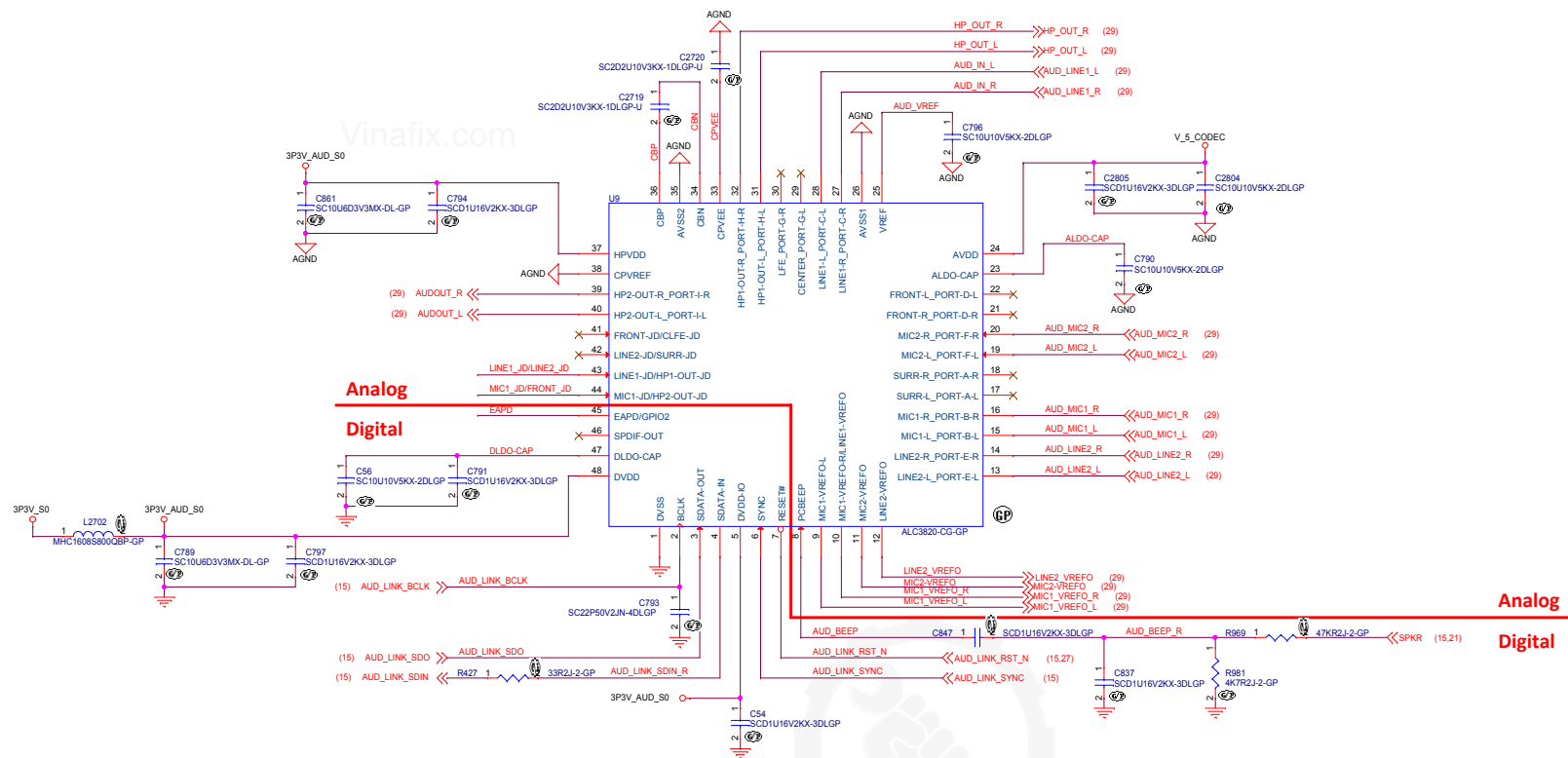


## Thermal sensor NCT7718W

The default value is trapping after power up 100ms by different pull-up resistors of T\_CRIT# and ALERT# pin:

TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125







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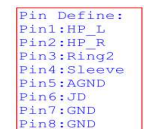
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iPhone, Samsung, Blackberry, HTC		
Pin Number	Pin Name	Description
1	Tip	Left Audio Out
2	Ring-1	Right Audio Out
3	Ring-2	Ground / Common
4	Sleeve	Microphone

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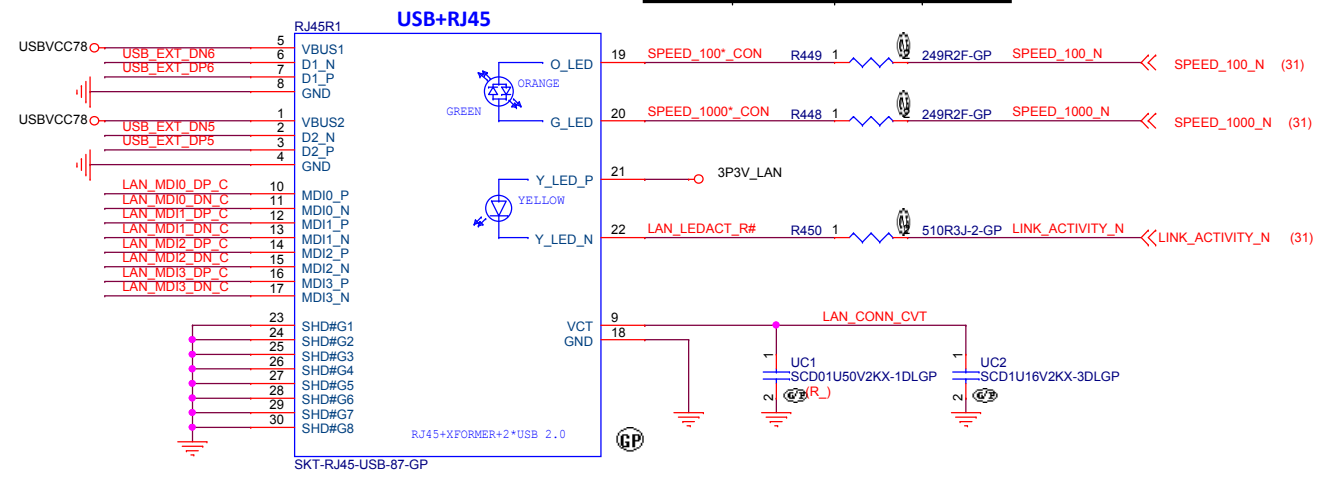
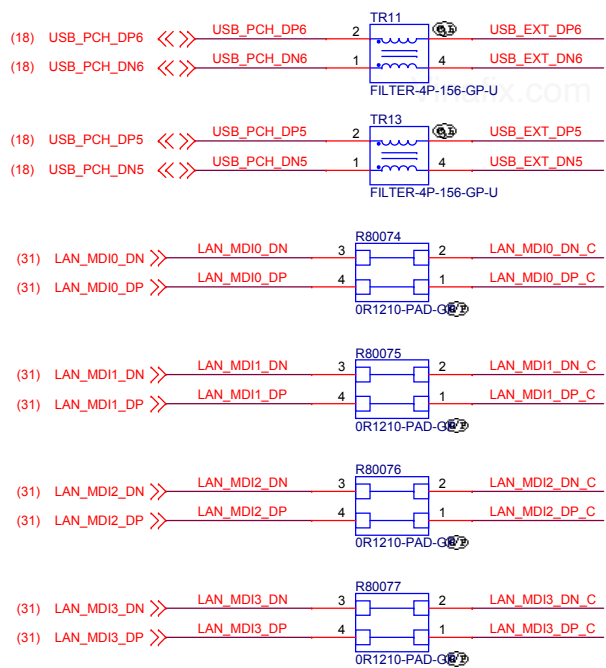
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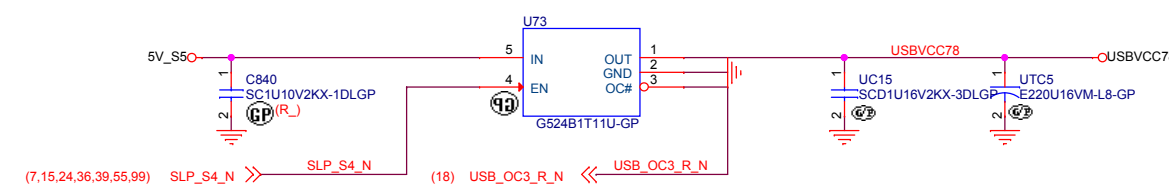
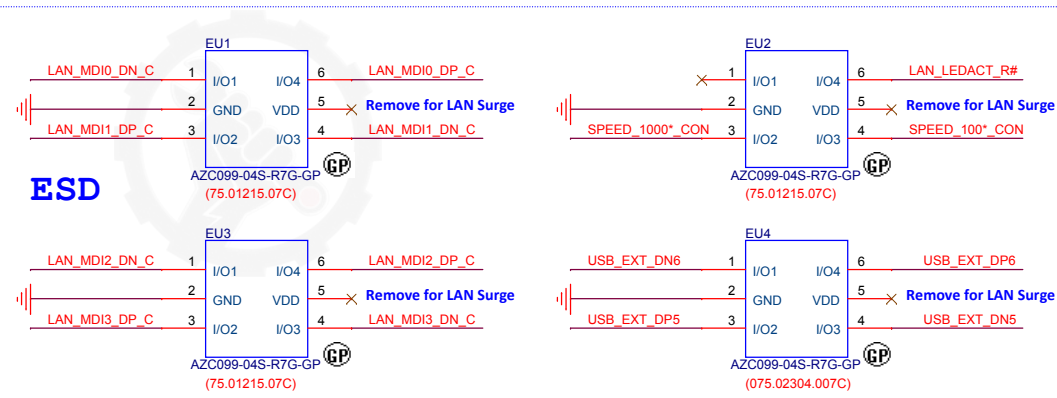
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	Giga	100M	10M
Link	Orange	Green	Green
Act	Blink	Blink	Blink



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Title <b>RJ45+USB2.0</b>		
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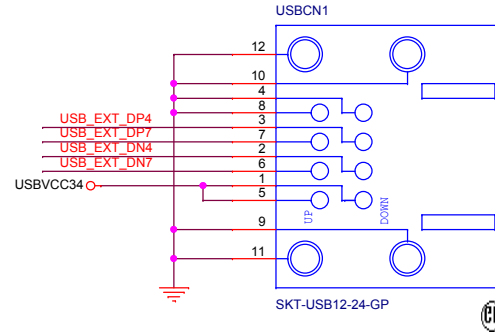
**Tahoe MT MLK/Gambits MT KBL**

Rev

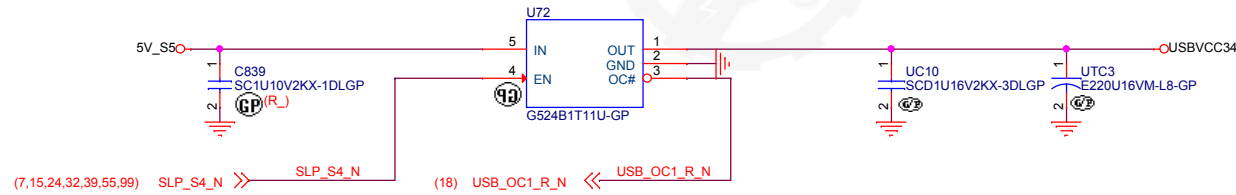
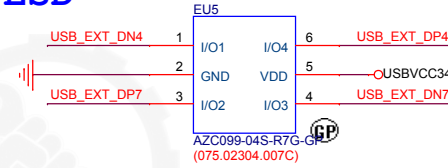
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### ESD



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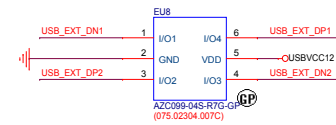
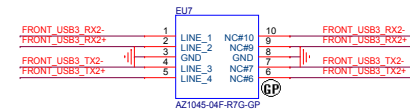
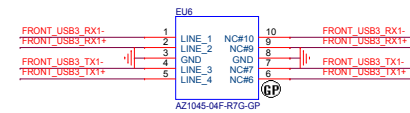
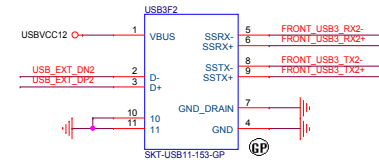
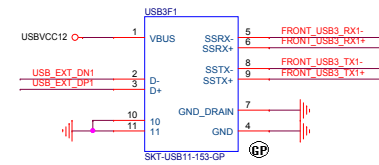
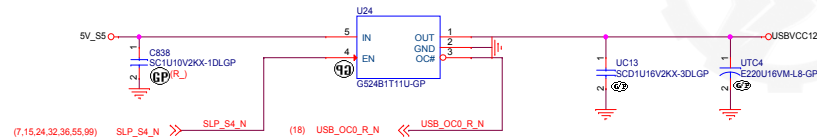
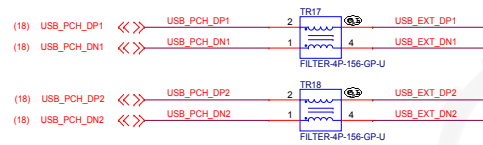
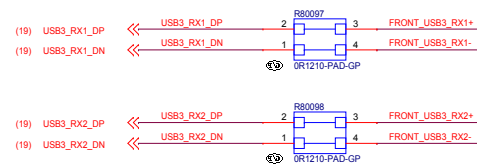
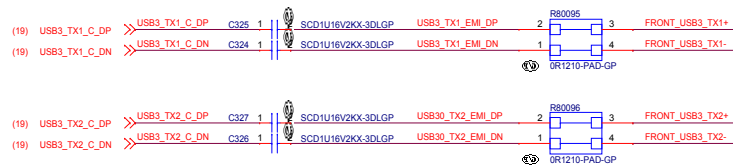
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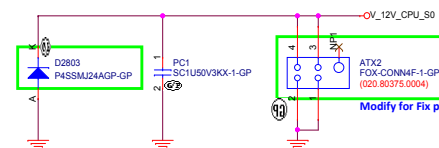
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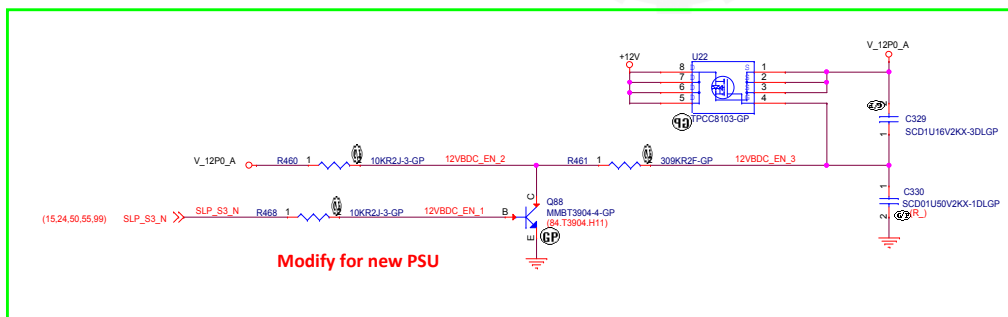
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The schematic diagram illustrates the power connections for the SATAP1 module. The module is represented by a blue rectangle with pins labeled NP1, 5, 2, 3, and NP2. It is connected to a 3P3V\_S0 power source, a +12V source, a +5V\_S0 source (highlighted in a green box), a 5V\_S0 source, and a +12V source. Capacitors C346 and C344 are shown connected to the 5V\_S0 and +12V sources respectively. The module is labeled SATAP1 and BAOT-CONN8-S1-GP.



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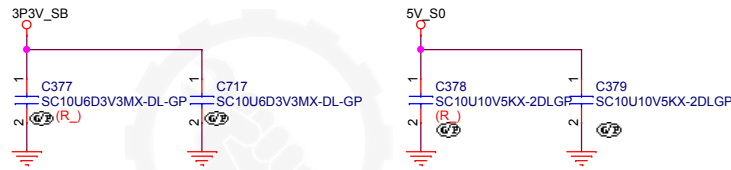
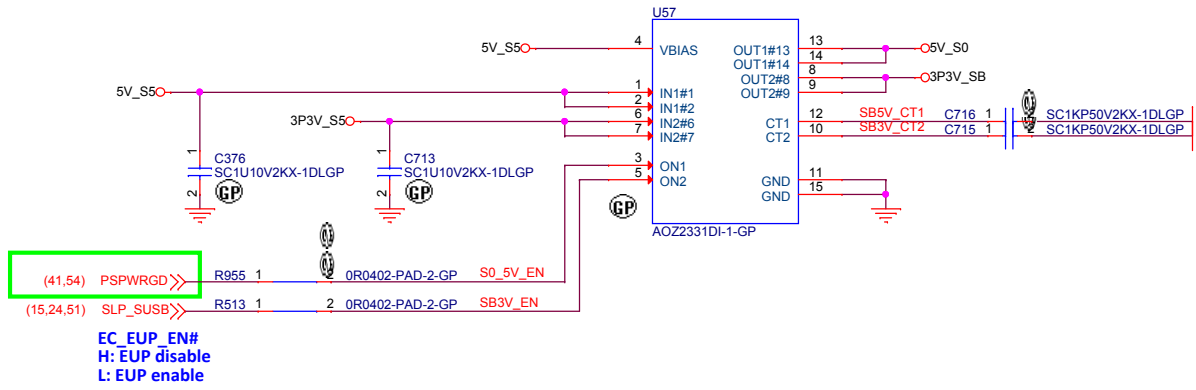
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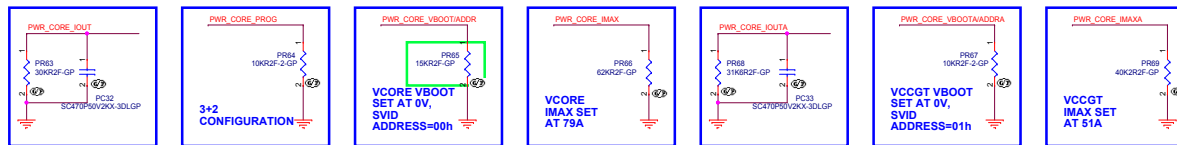
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# Intel SKYLAKE IMVP8 POWER CKT 3+2 PHASE

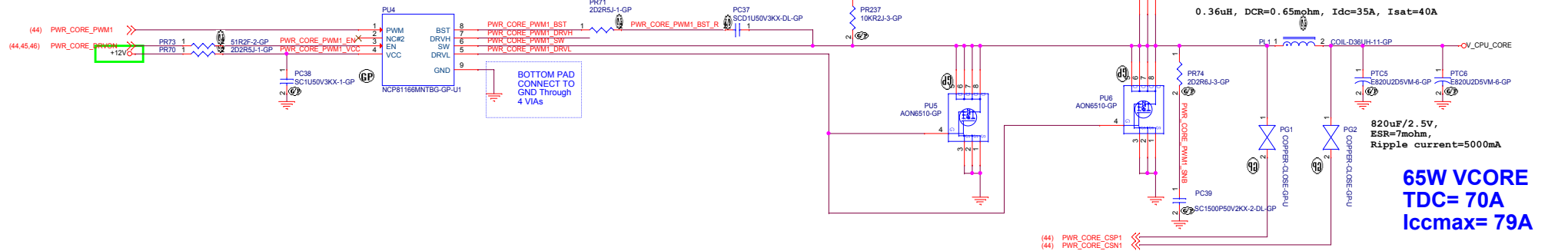


# VCC CORE&GT\_PWR

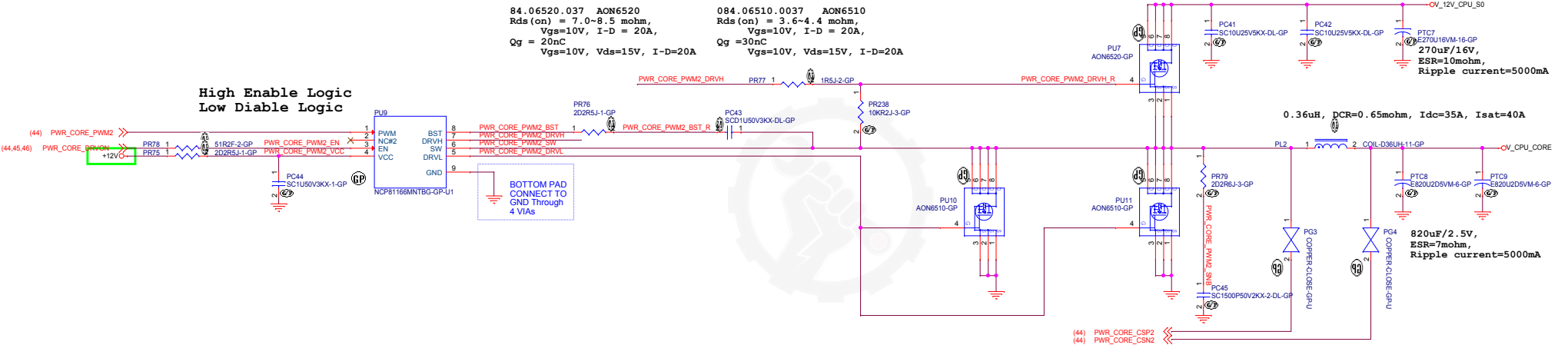
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Rds(on) = 7.0~8.5 mohm,  
Vgs=10V, I-D = 20A,  
Qg = 20nC  
Vgs=10V, Vds=15V, I-D=20A

084.06510.0037 AON6510  
Rds(on) = 3.6~4.4 mohm,  
Vgs=10V, I-D = 20A,  
Qg = 30nC  
Vgs=10V, Vds=15V, I-D=20A

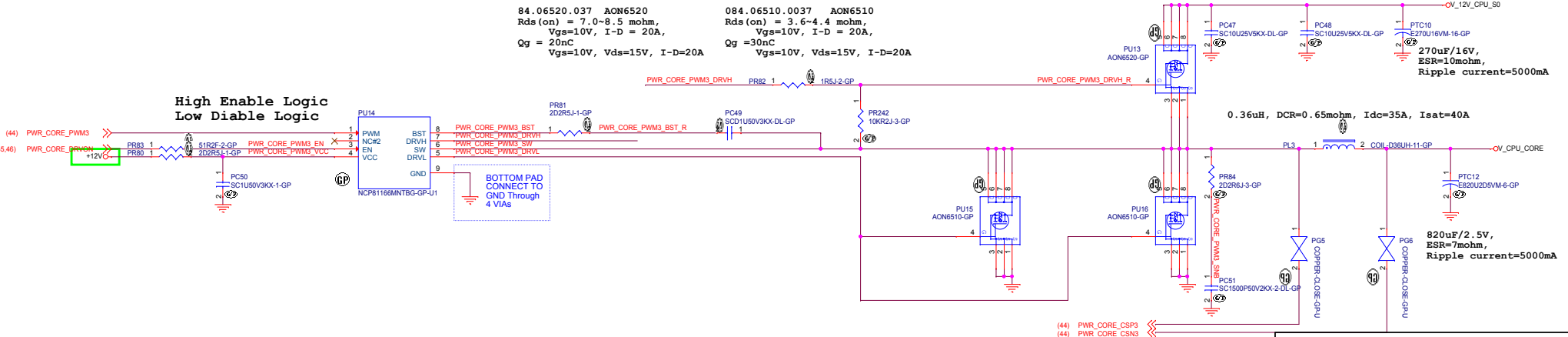
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High Enable Logic  
Low Diabie Logic



High Enable Logic  
Low Diabie Logic



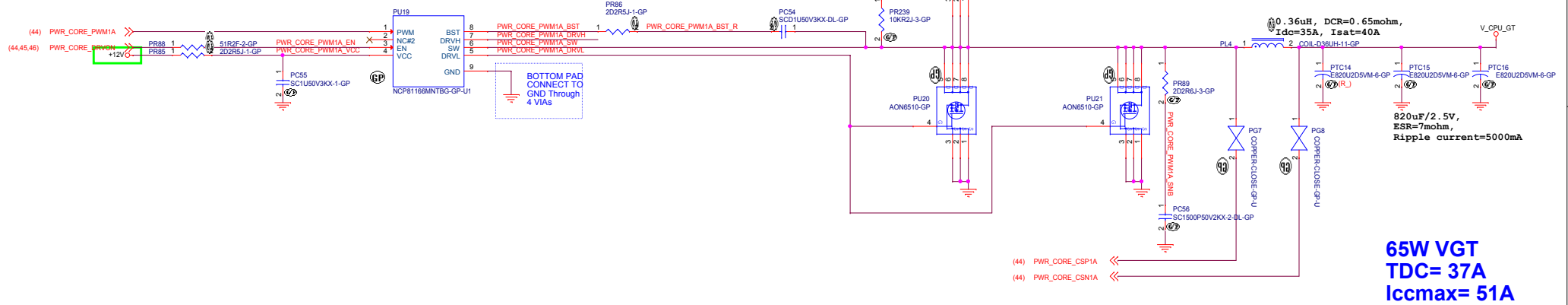
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# VCC CORE&GT\_PWR

84.06520.037 AON6520  
Rds(on) = 7.0~8.5 mohm,  
Vgs=10V, I-D = 20A,  
Qg = 20nC  
Vgs=10V, Vds=15V, I-D=20A

084.06510.0037 AON6510  
Rds(on) = 3.6~4.4 mohm,  
Vgs=10V, I-D = 20A,  
Qg = 30nC  
Vgs=10V, Vds=15V, I-D=20A

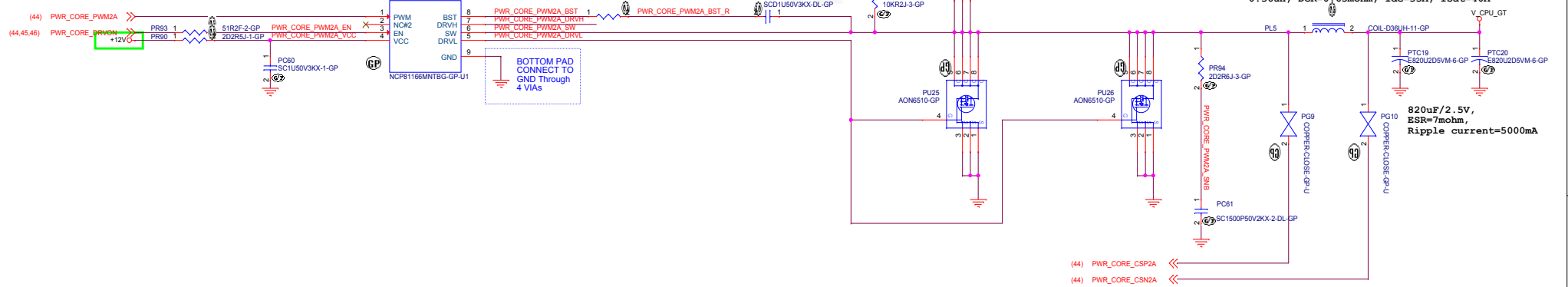
High Enable Logic  
Low Diabie Logic

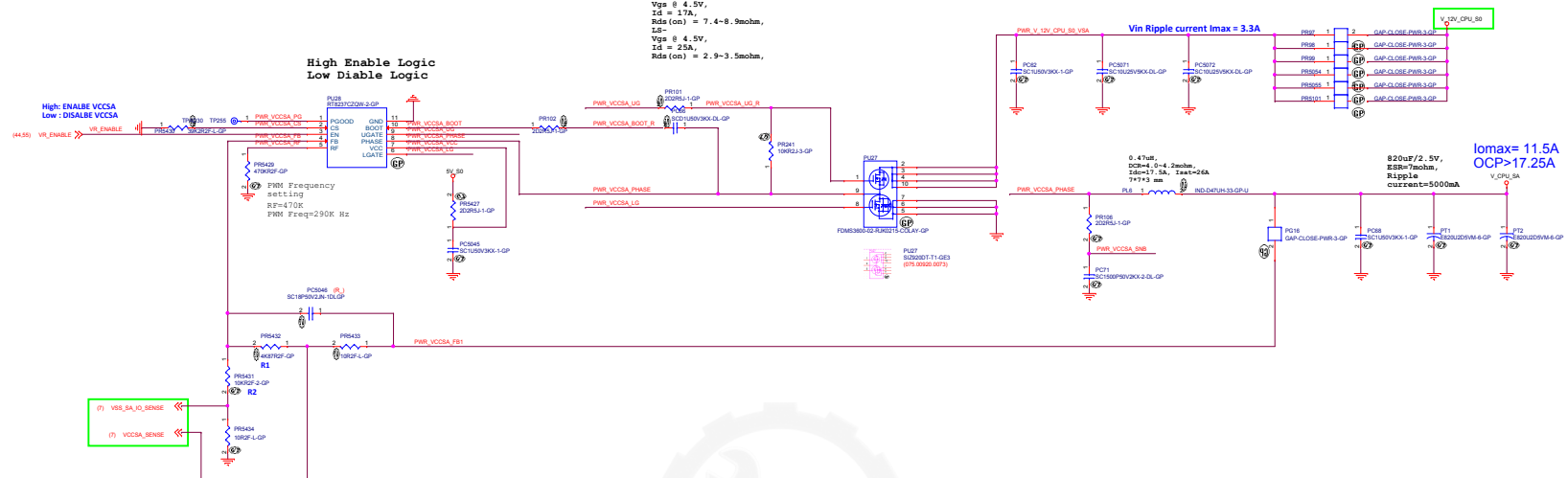


84.06520.037 AON6520  
Rds(on) = 7.0~8.5 mohm,  
Vgs=10V, I-D = 20A,  
Qg = 20nC  
Vgs=10V, Vds=15V, I-D=20A

084.06510.0037 AON6510  
Rds(on) = 3.6~4.4 mohm,  
Vgs=10V, I-D = 20A,  
Qg = 30nC  
Vgs=10V, Vds=15V, I-D=20A

High Enable Logic  
Low Diabie Logic









V\_5P0\_A

V\_3P3\_A

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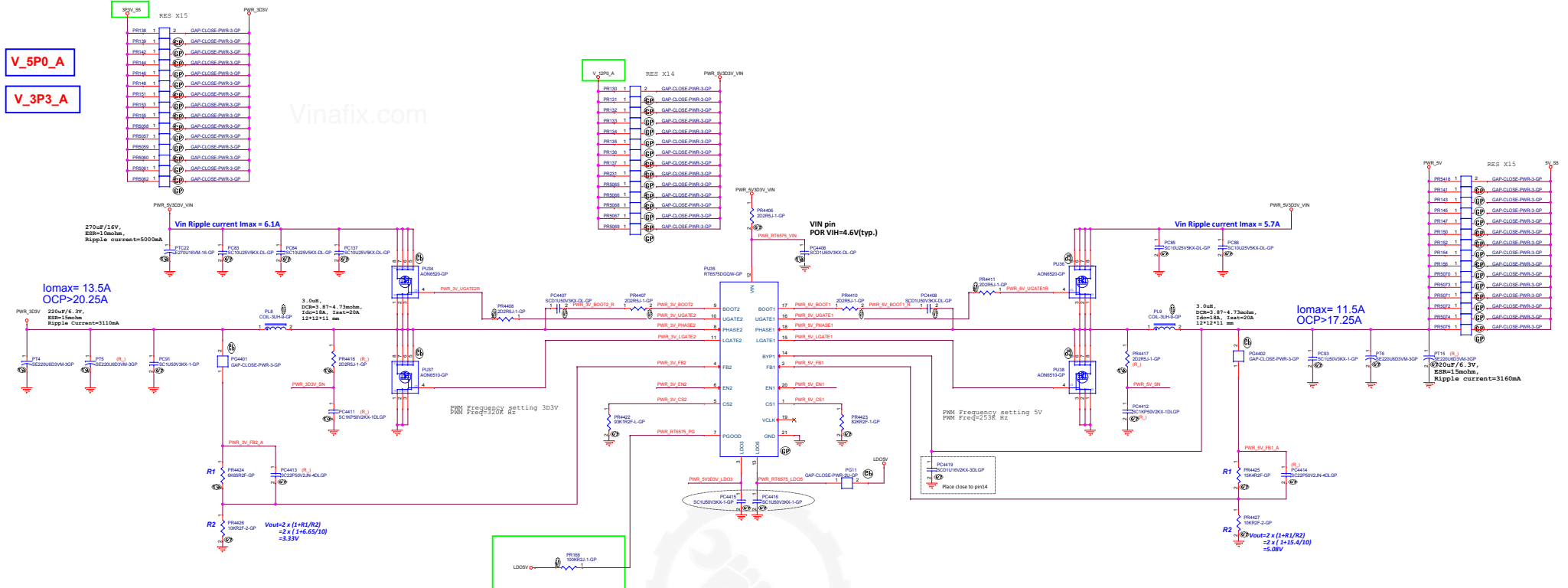
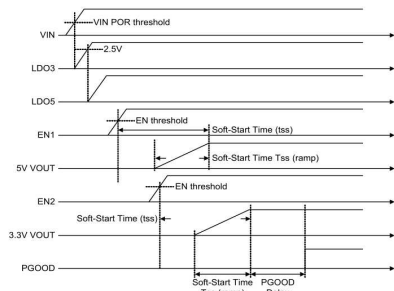


Figure 6. RT6575D Timing



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217, 4th, 5th, 6th, 7th, 8th, 9th, 10th, 11th, 12th, 13th, 14th, 15th, 16th, 17th, 18th, 19th, 20th, 21st, 22nd, 23rd, 24th, 25th, 26th, 27th, 28th, 29th, 30th, 31st, 32nd, 33rd, 34th, 35th, 36th, 37th, 38th, 39th, 40th, 41st, 42nd, 43rd, 44th, 45th, 46th, 47th, 48th, 49th, 50th, 51st, 52nd, 53rd, 54th, 55th, 56th, 57th, 58th, 59th, 60th, 61st, 62nd, 63rd, 64th, 65th, 66th, 67th, 68th, 69th, 70th, 71st, 72nd, 73rd, 74th, 75th, 76th, 77th, 78th, 79th, 80th, 81st, 82nd, 83rd, 84th, 85th, 86th, 87th, 88th, 89th, 90th, 91st, 92nd, 93rd, 94th, 95th, 96th, 97th, 98th, 99th, 100th

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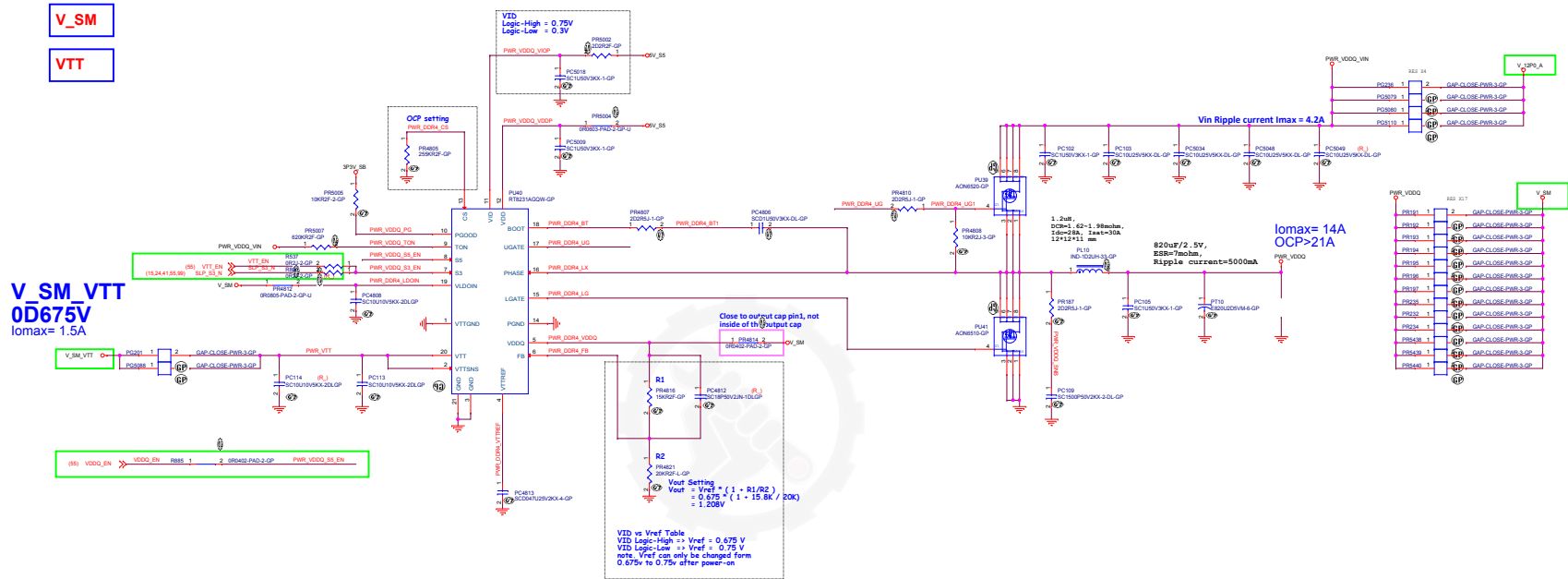
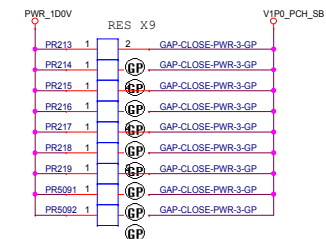
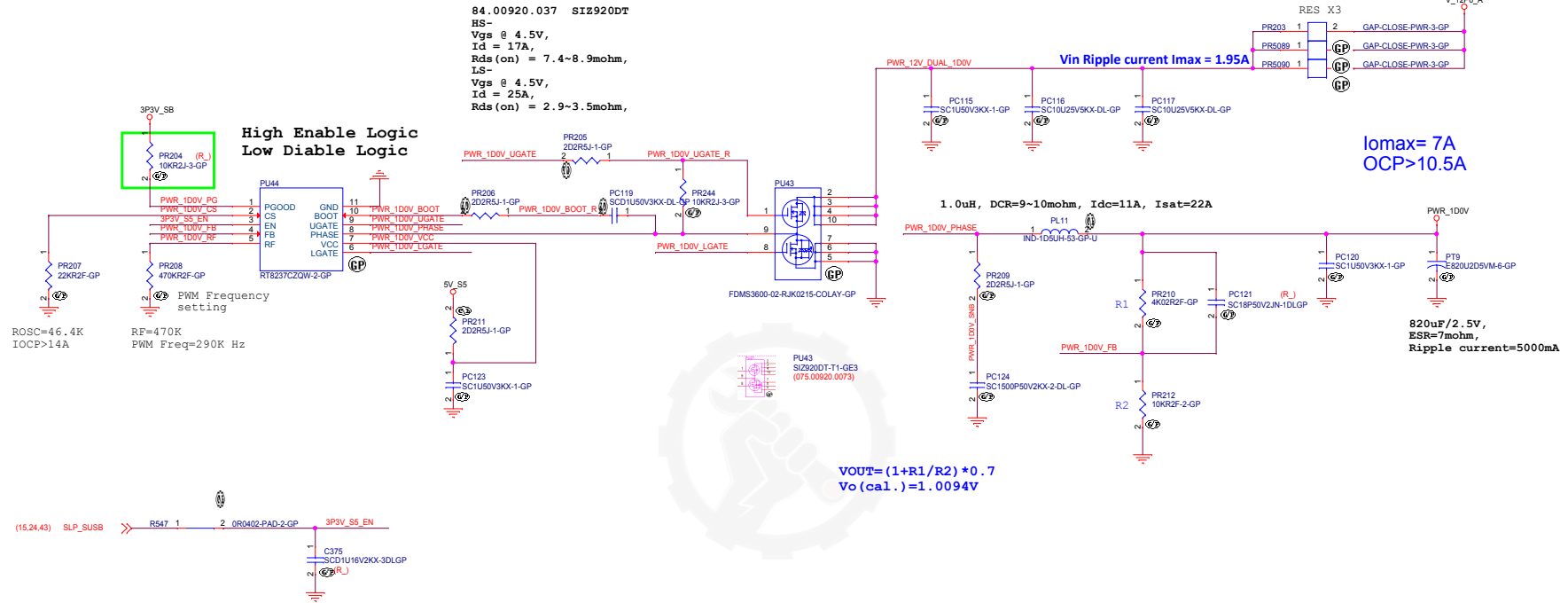


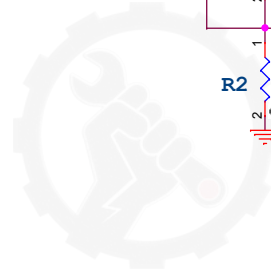
Table 2. S3 and S5 truth table

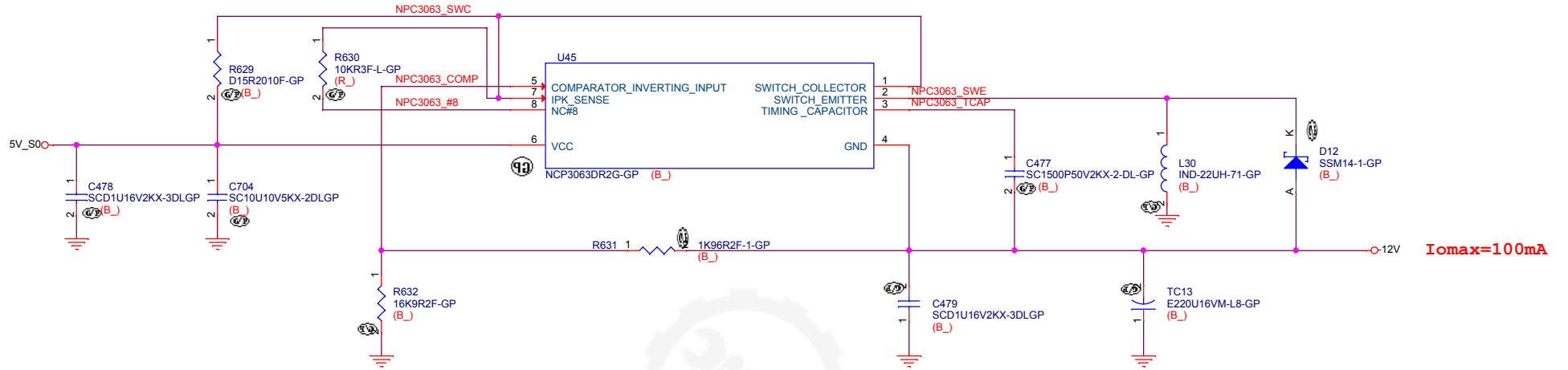
STATE	S3	S5	VDDQ	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

Table 1. VID and Reference Voltage Setting

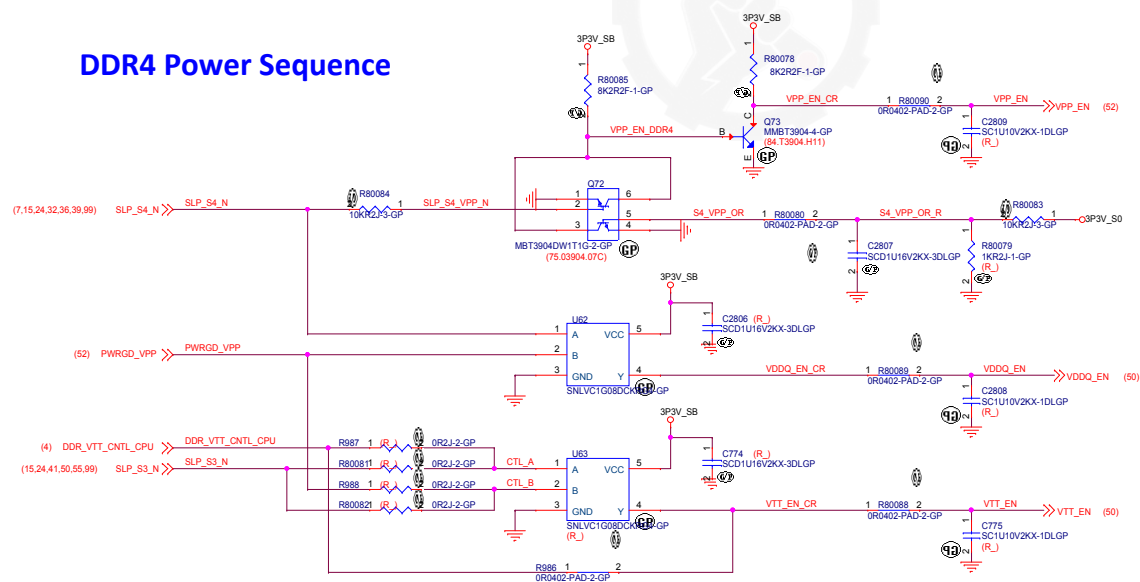
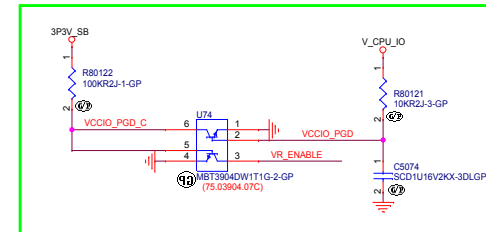
VID	Reference Voltage (V)
High	0.675
Low	0.75

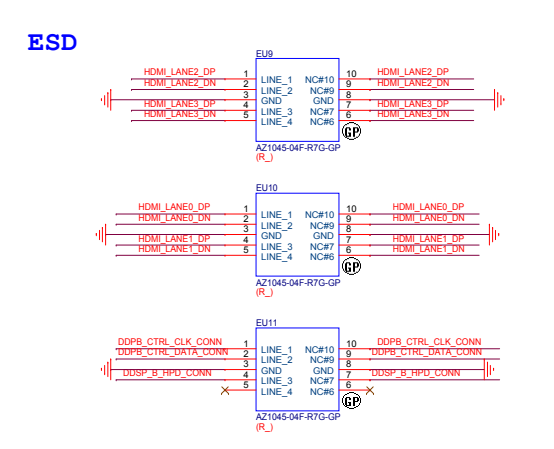
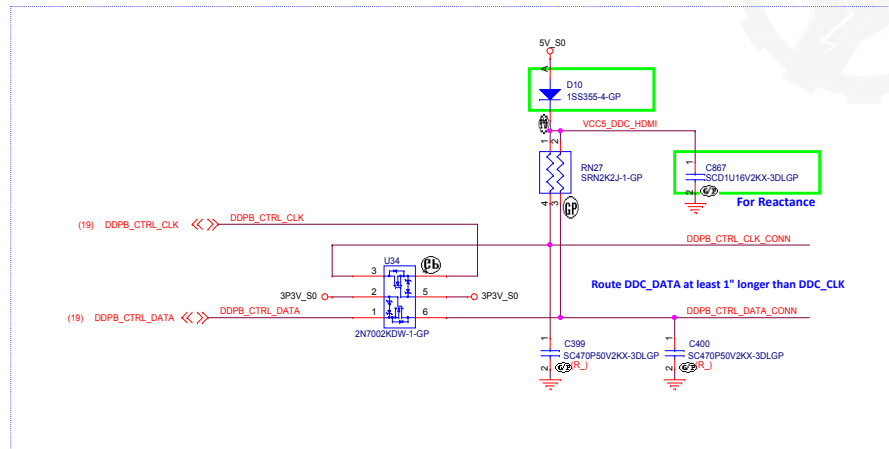
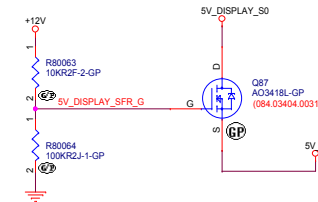
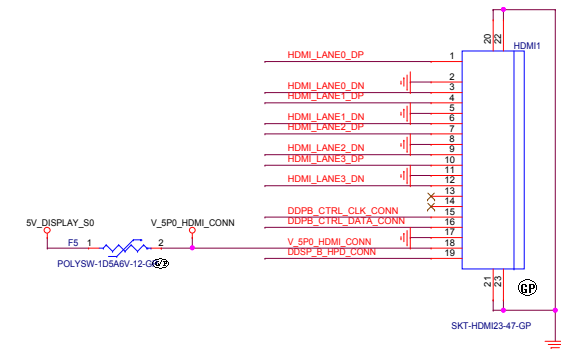
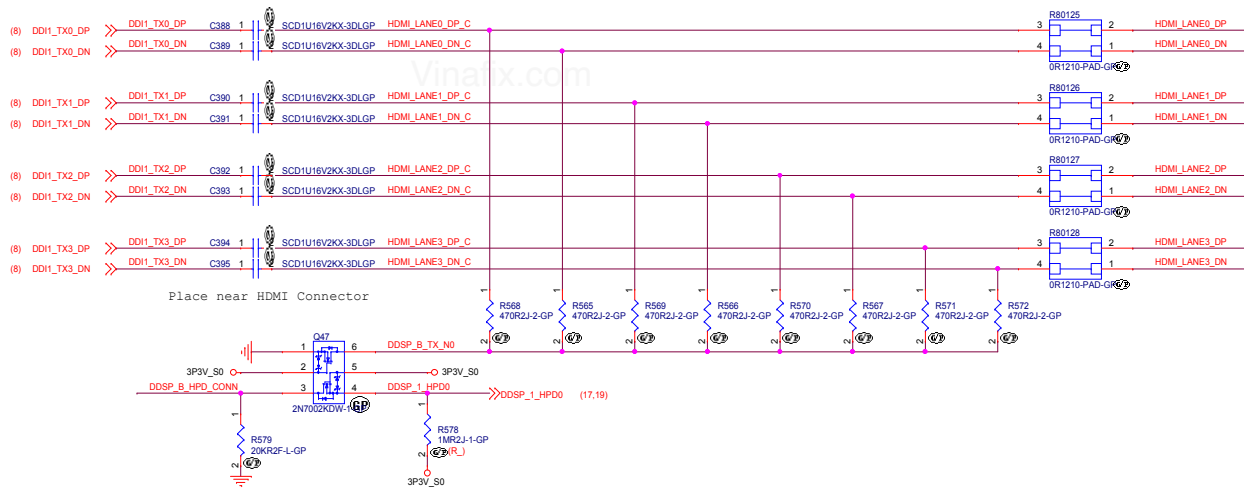














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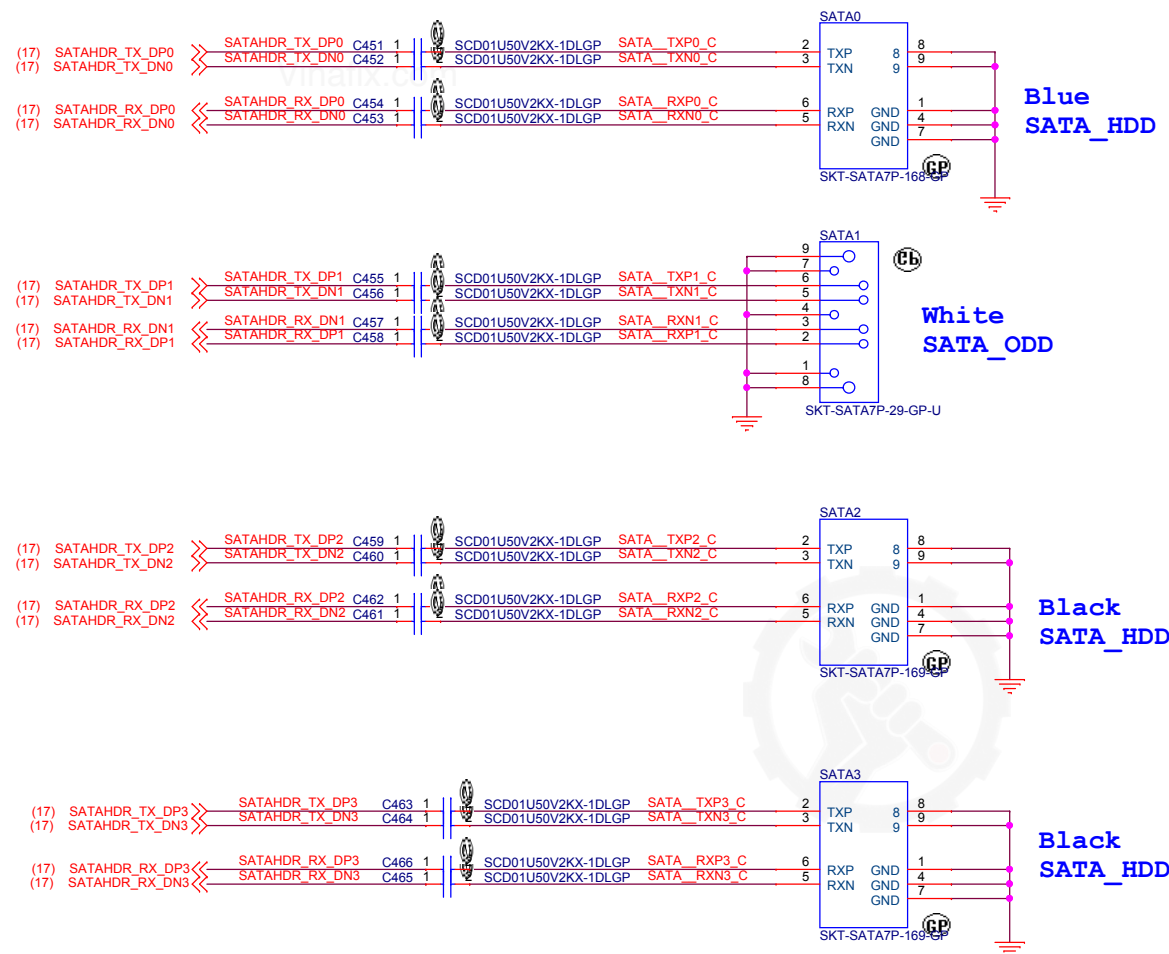
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Date:

Wednesday, October 19, 2016

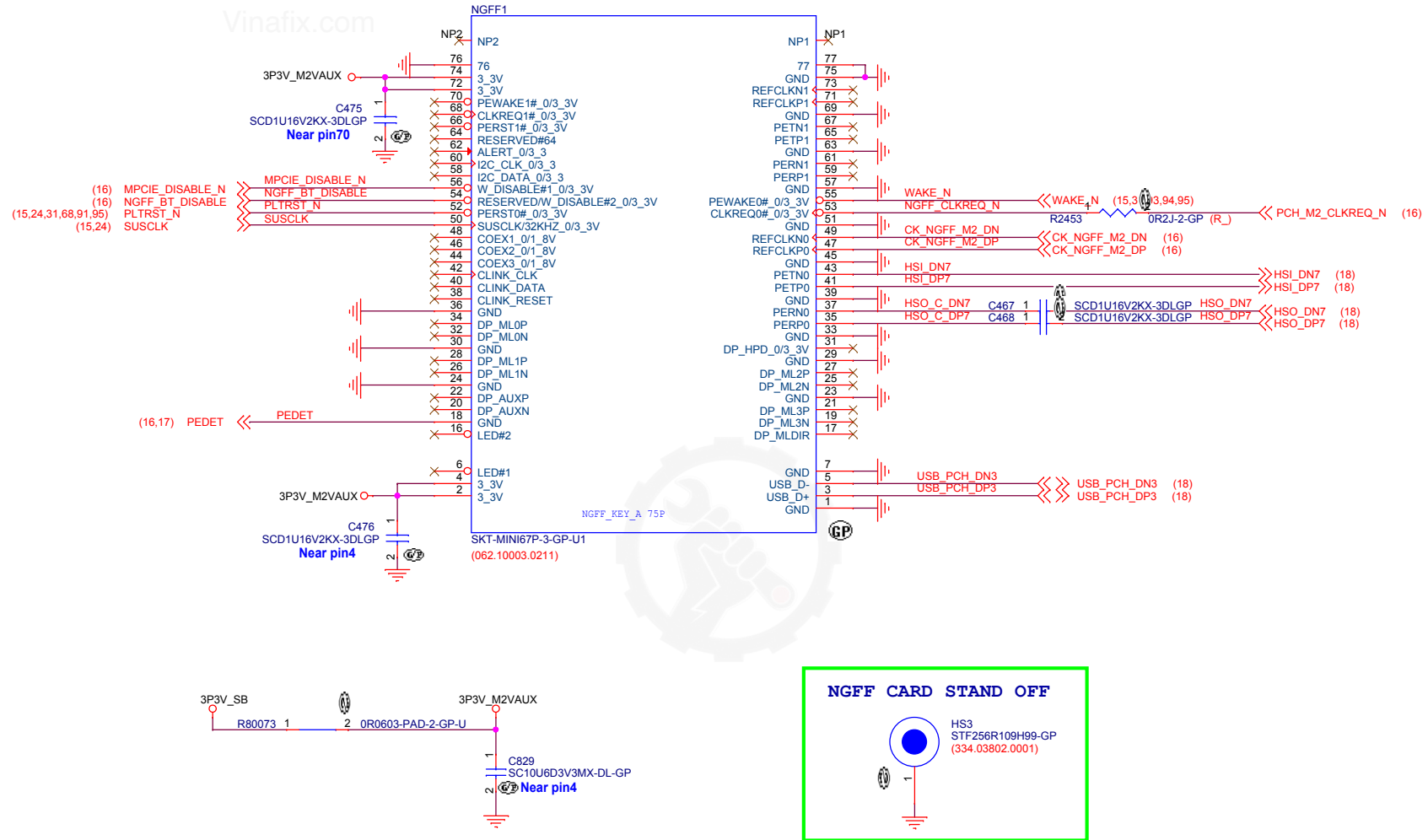
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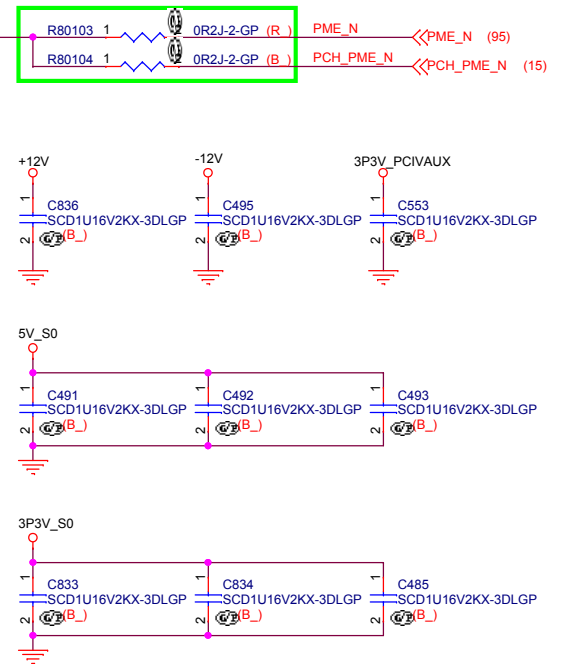
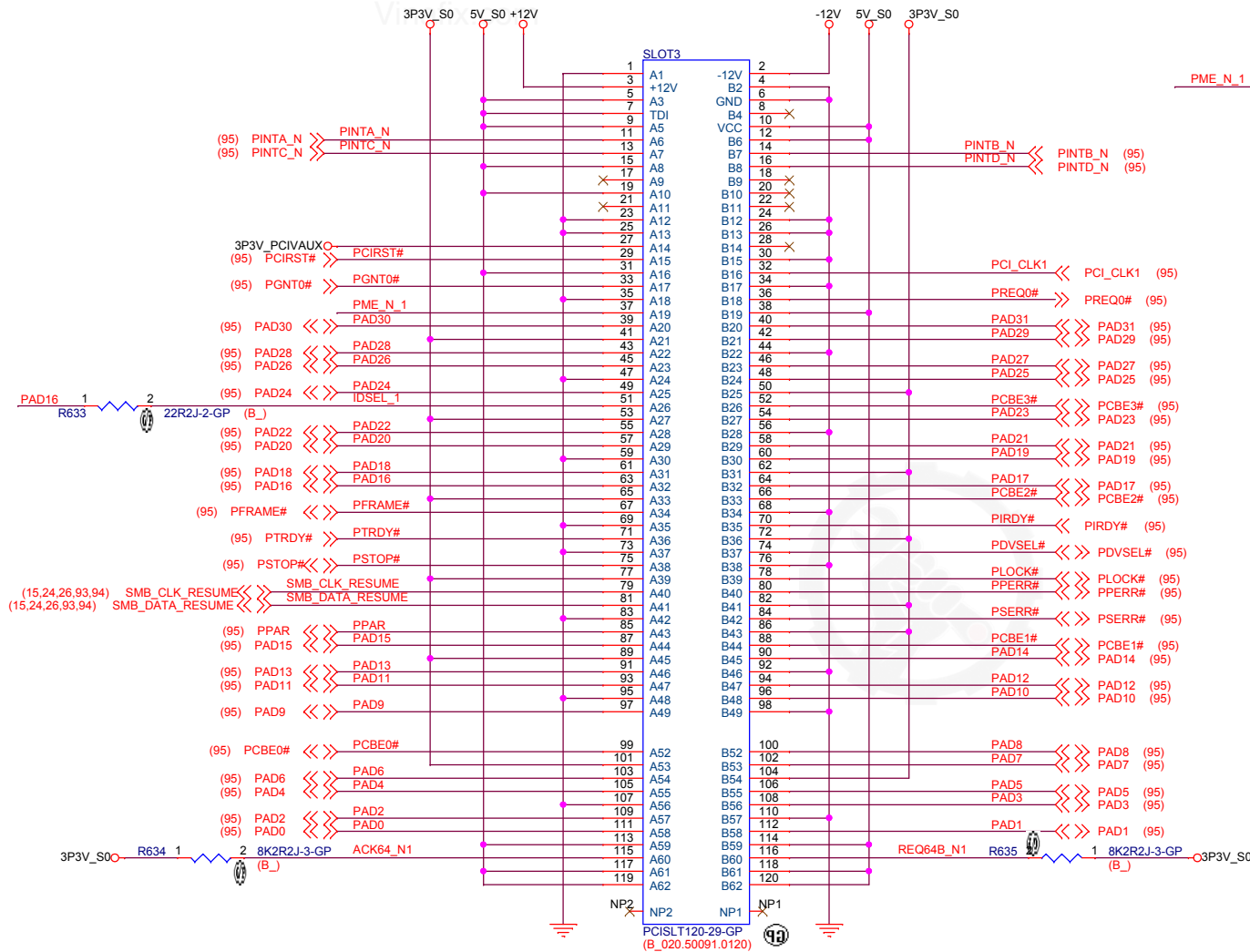
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H: 4.2mm

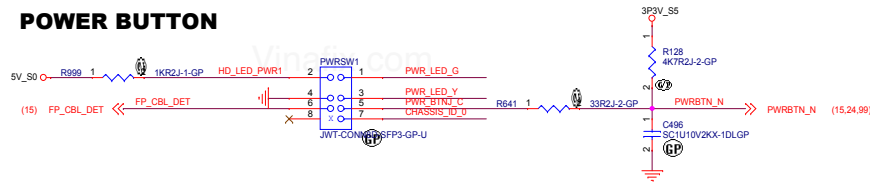




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Title <b>PCI Slot</b>		
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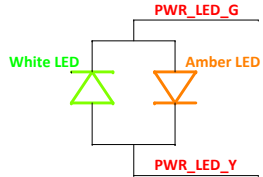
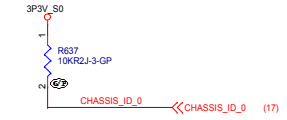
## POWER BUTTON



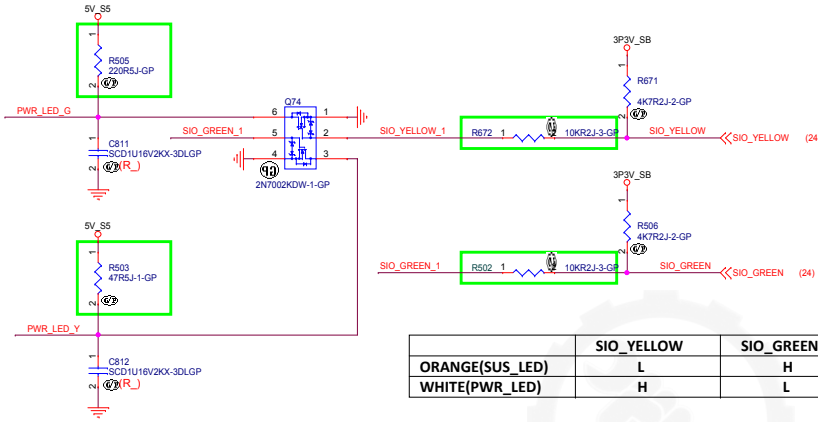
## Chassis ID

ID_0	Chassis	CY16 (KBL)	CY15 (SKL)
0	Vostro	Tahoe MLK	Tahoe
1	Inspiron	Gambits	Lotus

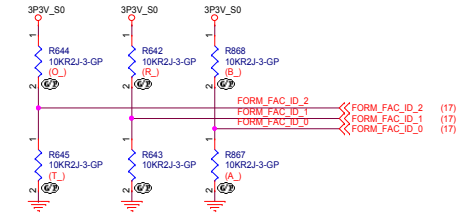
Power switch cable select



S0	White
S3	White(blinking)
S4/S5	LED off
No Post	Amber
Failure to Post	Amber(blinking)

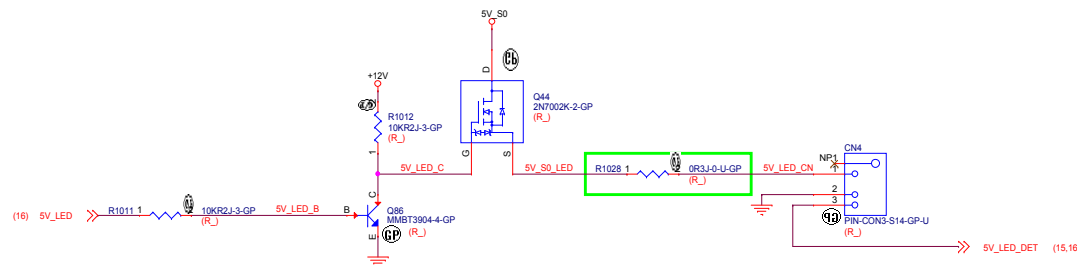
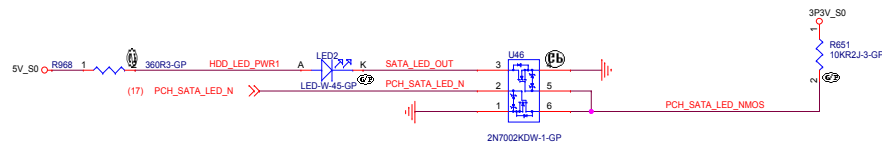


	SIO_YELLOW	SIO_GREEN
ORANGE(SUS_LED)	L	H
WHITE(PWR_LED)	H	L



## SKU ID

Type	ID_2	ID_1	ID_0
Tahoe MT MLK with TPM	0	0	0
Tahoe MT MLK w/o TPM	1	0	0
Tahoe CBB MT MLK with TPM	0	0	1
Tahoe CBB MT MLK w/o TPM	1	0	1
Tahoe SFF MLK with TPM	0	1	1
Tahoe SFF MLK w/o TPM	1	1	1





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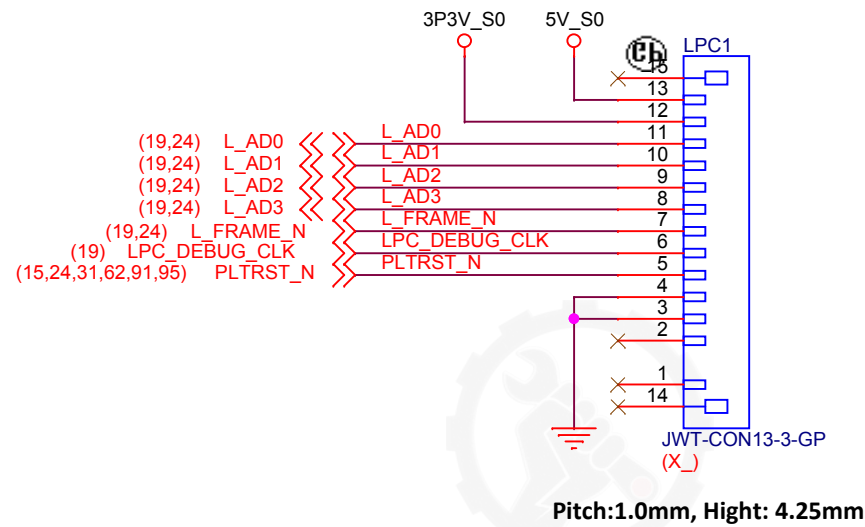
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# LPC DEBUG PORT



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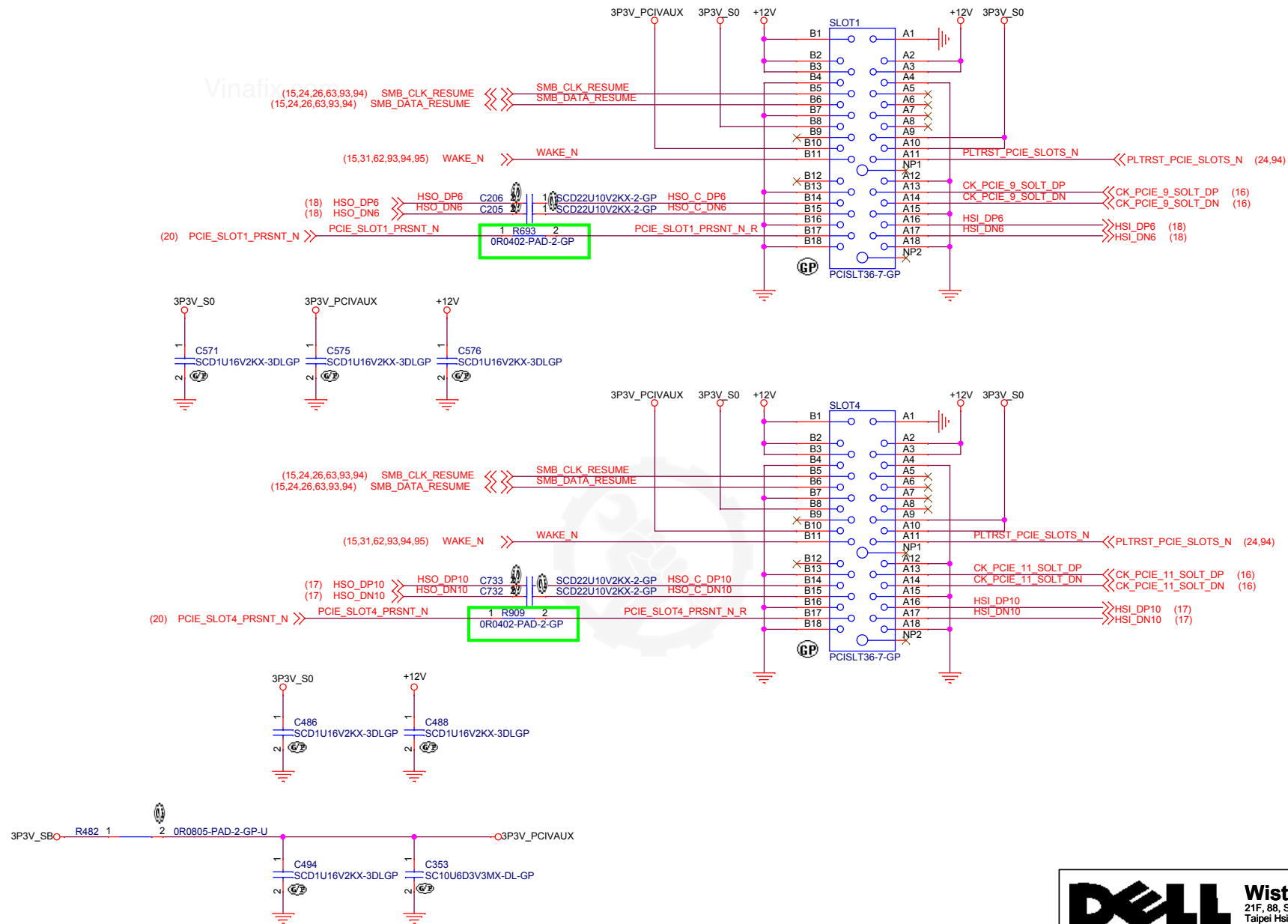
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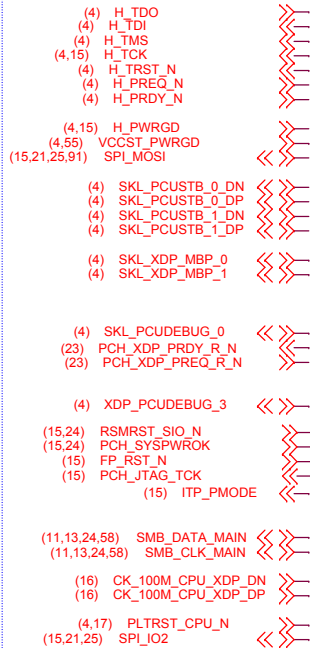
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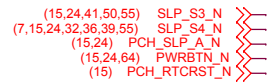
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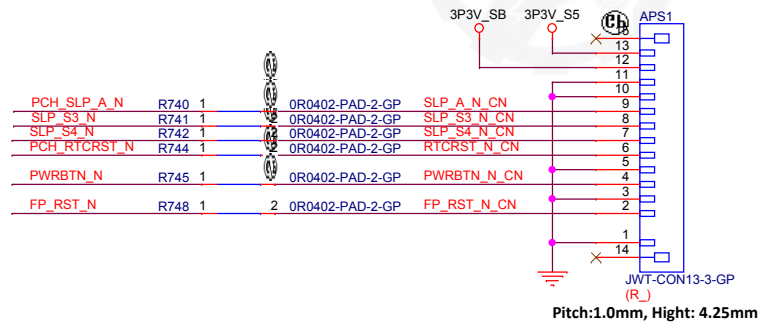
## XDP for CPU



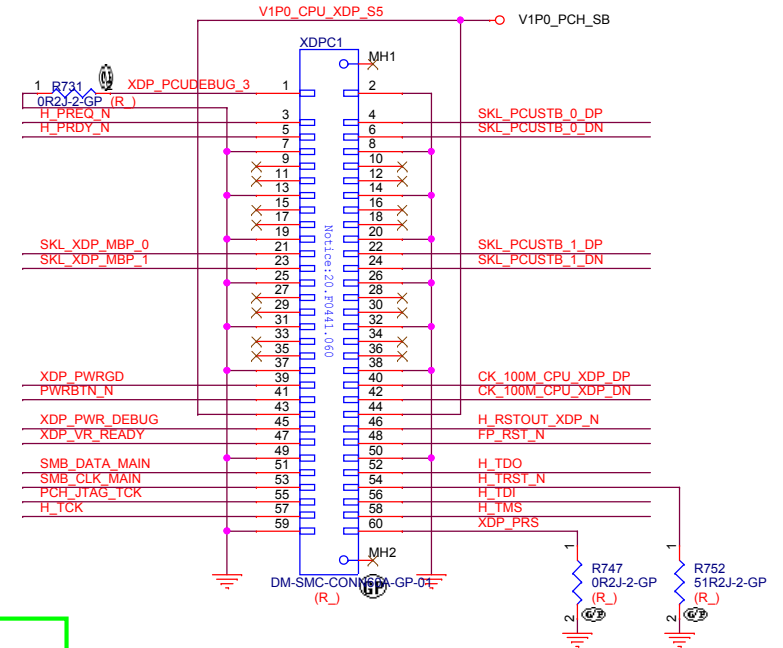
## APS DEBUG



## APS CONNECTOR



## XDP for CPU



Layout Notes

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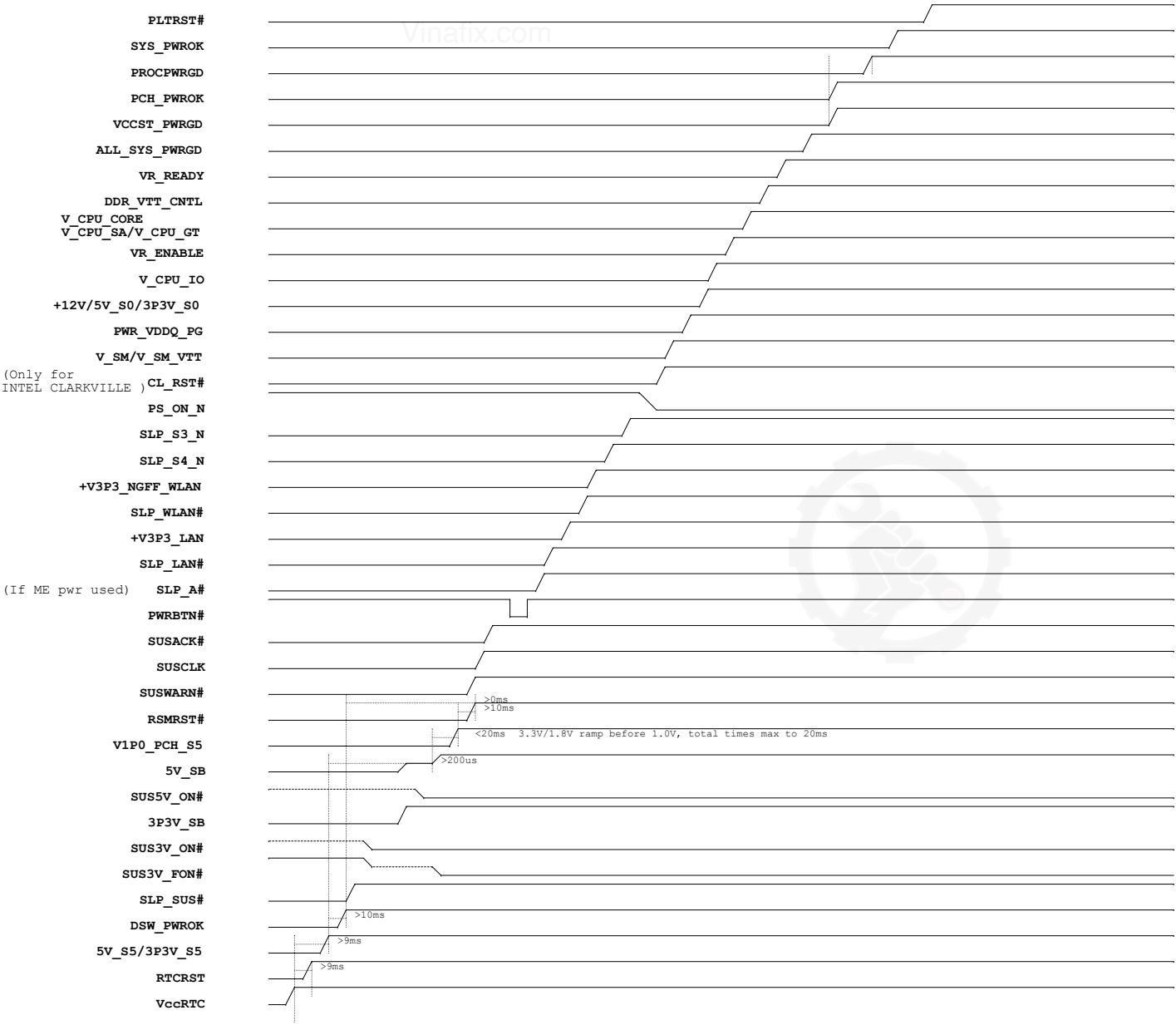
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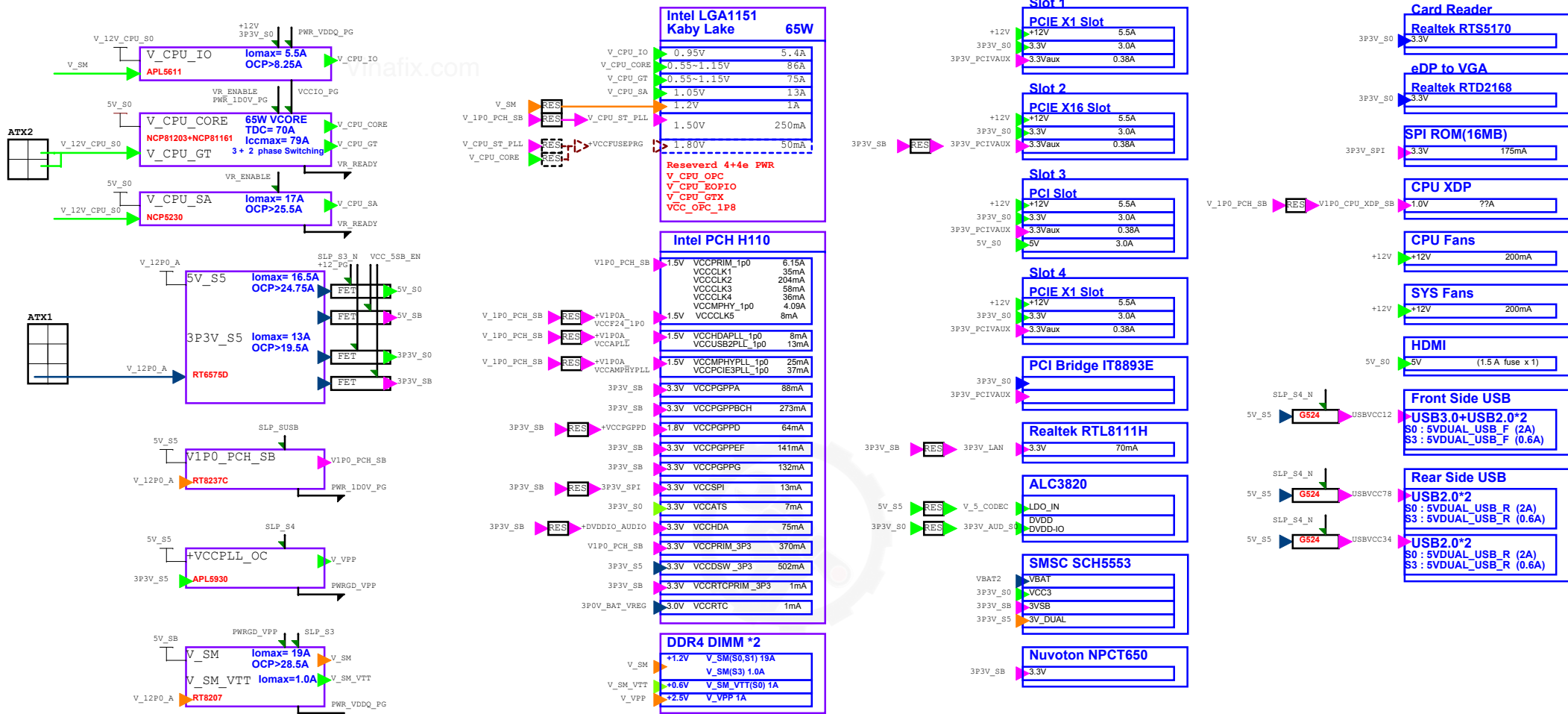
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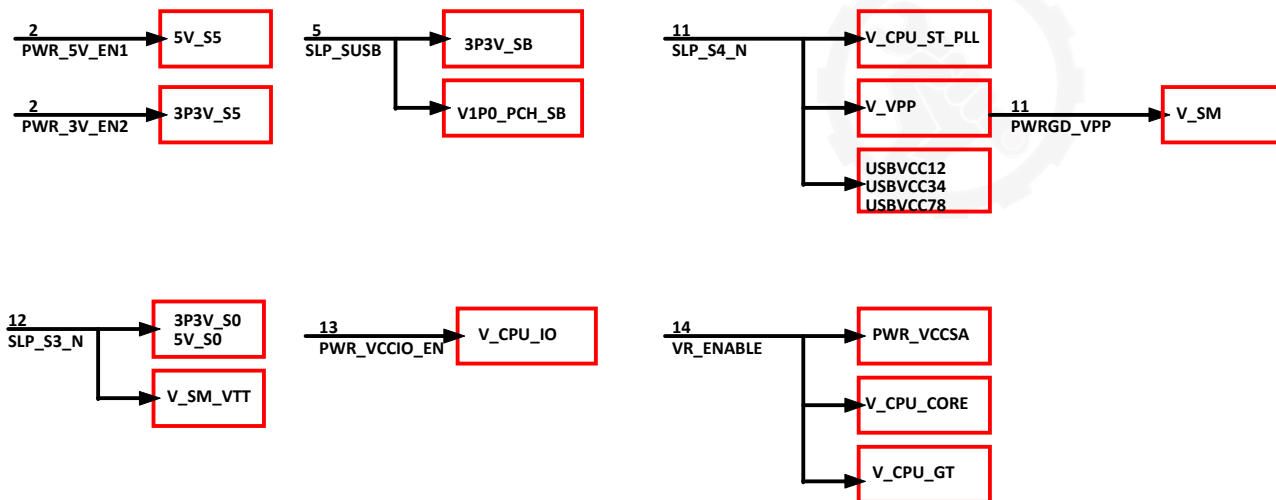
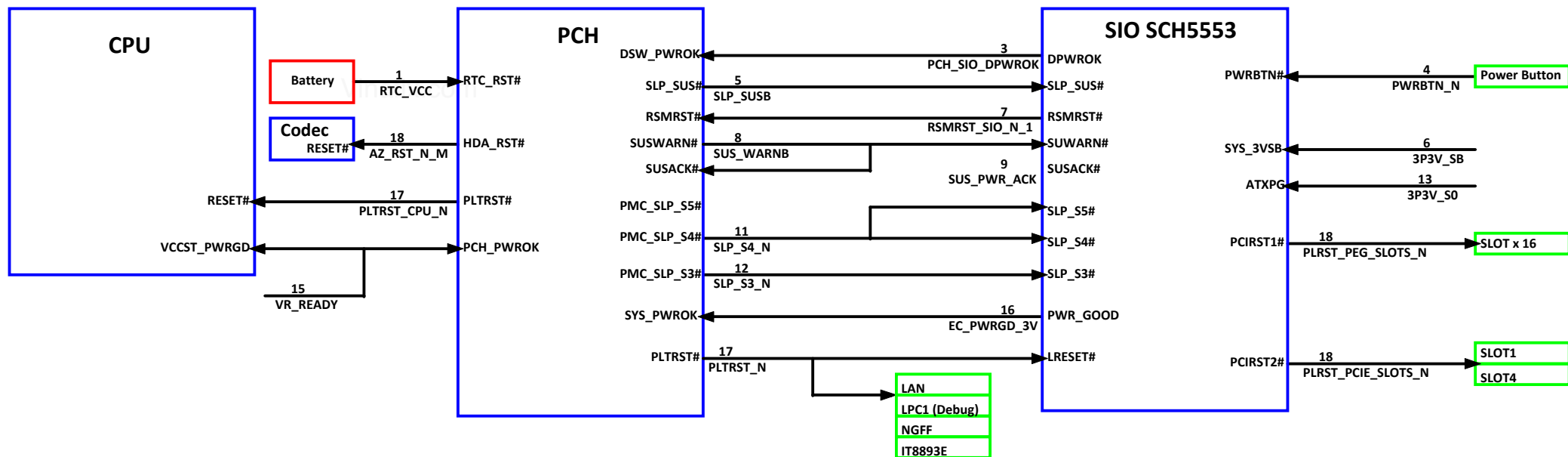
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POWER ON SEQUENCE









SLOT4 SLOT3 SLOT2 SLOT1

INTEL  
Kaby Lake-S  
(65W 4C + GT2)

SKT H4 LGA1151  
42.5 mm x 42.5 mm



Channel A  
2133MHz/2400MHz

DDR4 DIMM  
Unbuffered 8GB

Channel B  
2133MHz/2400MHz

DDR4 DIMM  
Unbuffered 8GB

1 2 3

INTEL PCH  
Skylake  
PCH-H

FCBGA 837PIN  
23 mm x 23 mm



100MHz

Realtek Lan  
RTL8111H

25MHz

100MHz

CPU XDP

PCH XDP

100MHz

ITE IT8893E

33MHz

100MHz

NGFF

24MHz

LPC 80 Port

24MHz

SIO  
SMSC SCH5553

24MHz

24MHz

32.768KHz

32.768KHz

	Name	Type	SSC Capable	Description
	CLKOUT_ITPXPDP_P CLKOUT_ITPXPDP_N	O	Yes	Differential ITP Debug Clock: 100 MHz differential output to processor XDP/ITP connector on the platform
1	CLKOUT_CPUNSSC_P CLKOUT_CPUNSSC_N	O	No	Unfiltered Clock from Crystal to CPU: 24 MHz differential re-buffered crystal reference clock to the processor
2	CLKOUT_CPUPCIBCLK_P CLKOUT_CPUPCIBCLK_N	O	Yes	Differential PCIe* Reference Clock to CPU: 100 MHz PCIe* 3.0 specification compliant differential PCIe* reference clock to the processor
3	CLKOUT_CPUBCLK_P CLKOUT_CPUBCLK_N	O	Yes	Differential Clock to CPU: 100 MHz differential core reference clock to the processor
	CLKOUT_SRC_P[15:0] CLKOUT_SRC_N[15:0]	O	Yes	PCI Express* Clock Output: 100 MHz PCIe* 3.0 specification compliant differential output clocks to PCIe* devices
	CLKOUT_LPC[1:0]	O	No	LPC Clock Outputs: Single-Ended 24 MHz output to various single load connectors/devices
	CLKOUT_48	O	No	48 Clock Output (SKL-H Server Only): Single-Ended 48 MHz output to Server BMC devices
	SRCLCKRQ#[15:0]	I/O	N/A	Clock Request: Clock request signals for PCIe* 100 MHz differential clocks
	XTAL24_IN	I	N/A	Crystal Input: Input connection for 24 MHz crystal to PCH oscillator circuit
	XTAL24_OUT	O	N/A	Crystal Output: Output connection for 24 MHz crystal to PCH oscillator circuit

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**REST Flow Chart**

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